

# COMPAL CONFIDENTIAL

MODEL NAME : QAR10

PCB NO : LA-7933P

BOM P/N : 4319FV31L01

GPIO MAP: E4 VC GPIO map rev 1.1

## Vans 17

REV : 0.2 (X01)

2011.11.11

[www.aitech1.ru](http://www.aitech1.ru)

@ : Nopop Component

CONN@ : Connector Component

PXDP@: PCH XDP Component

MB Type	BOM P/N		
TPM EN/ TCM DIS		1@	3@
TPM DIS/ TCM EN		2@	3@
TPM DIS/ TCM DIS		2@	4@

### MB PCB

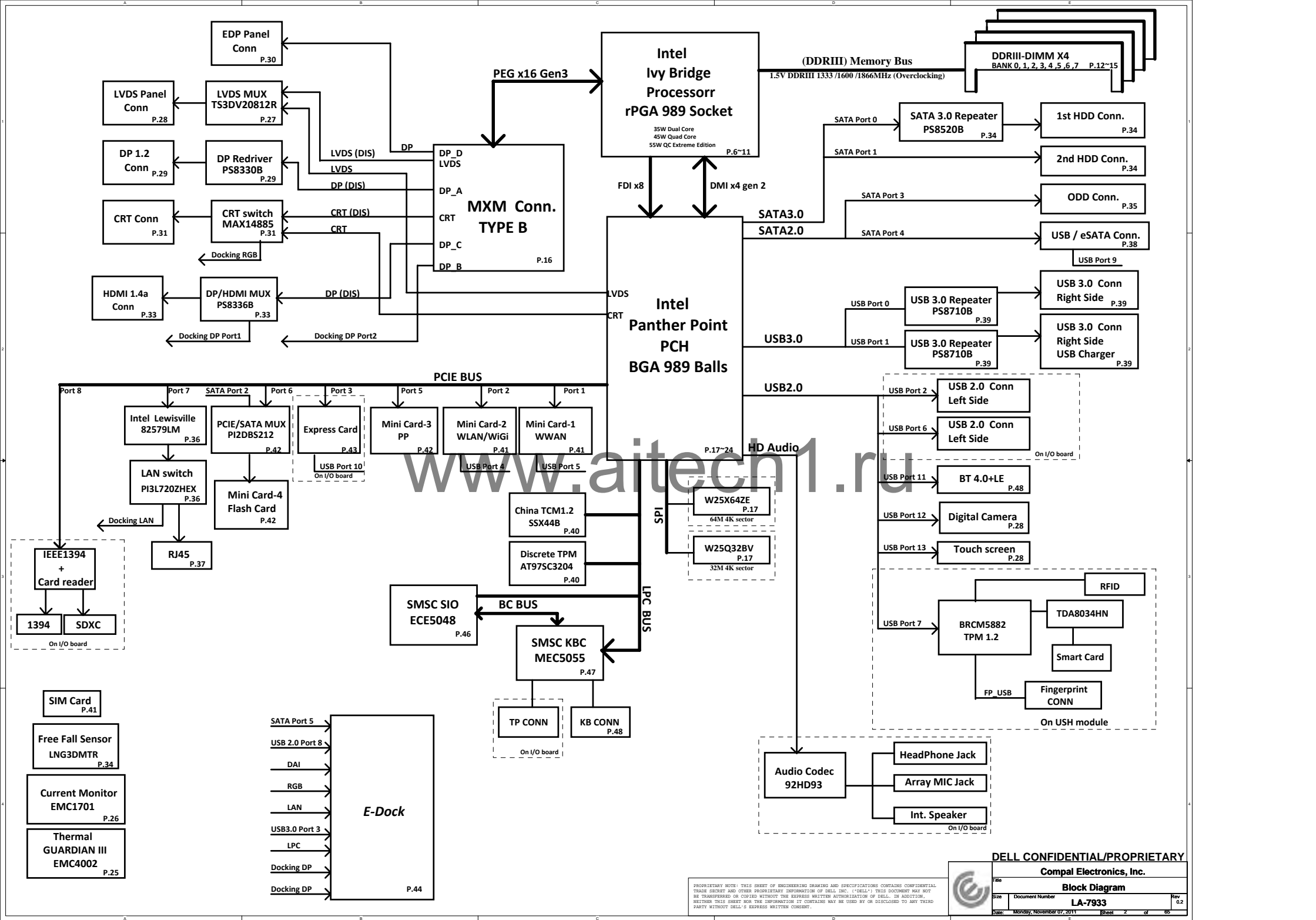
Part Number	Description
DAA00002U00	PCB OMF LA-7933P REVO MB

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Cover Sheet			
Title	LA-7933		
Size	Document Number	Rev	0.2
Date: Friday, November 11, 2011	Sheet 1	of	65



POWER STATES

Signal State	SLP S3#	SLP S4#	SLP S5#	S4 STATE#	SLP M#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3 (Suspend to RAM) / M1	LOW	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M1	LOW	LOW	HIGH	LOW	HIGH	ON	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M1	LOW	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF	OFF
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

PM TABLE

power plane State	+15V_ALW +5V_ALW +3.3V_ALW_PCH +3.3V_RTC_LDO	+3.3V_SUS +1.5V_MEM	+5V_RUN +3.3V_RUN +1.8V_RUN +1.5V_RUN +0.75V_DDR_VTT +VCC_CORE +1.05V_RUN_VTT +1.05V_RUN	+3.3V_M +1.05V_M	+3.3V_M +1.05V_M (M-OFF)
S0	ON	ON	ON	ON	ON
S3	ON	ON	OFF	ON	OFF
S5 S4/AC	ON	OFF	OFF	ON	OFF
S5 S4/AC don't exist	OFF	OFF	OFF	OFF	OFF

Stack up

Layer No.	Name	Er	Material	Thickness (Material SPEC.) Unit : mil
			SolderMask	IT-158
			Add Plating	
1	Top		Copper foil	0.5oz
		3.7	Prepreg	1080
2	Core 1		Copper foil	1oz
		3.7	Core	4mil
3	Sig 1		Copper foil	1oz
		3.9	Prepreg	1080Hx2116H
4	Core/PWR		Copper foil	2oz
		3.7	Core	4mil
5	Sig 2		Copper foil	1oz
		3.8	Prepreg	1080Hx2
6	Sig 3		Copper foil	1oz
		3.7	Core	4mil
7	Core/PWR		Copper foil	2oz
		3.9	Prepreg	1080Hx2116H
8	Sig 4		Copper foil	1oz
		3.7	Core	4mil
9	Core 3		Copper foil	1oz
		3.7	Prepreg	1080
10	Bottom		Copper foil	0.5oz
			Add Plating	
			SolderMask	57.09
Overall Thickness (1.45mm ± 10%)				

SATA	DESTINATION
SATA 0	HDD 1
SATA 1	HDD 2
SATA 2	NVRAM
SATA 3	ODD
SATA 4	ESATA
SATA 5	Dock

PCH	USB PORT#	DESTINATION
	0	JUSB1 (Ext Right Side)
	1	JUSB2 (Ext Right Side)
	2	IO Board- JUSB1 (Ext Left Side)
	3	Docking USB3.0
	4	WLAN
	5	WWAN
	6	IO Board- JUSB2 (Ext Left Side)
	7	USH
	8	Docking USB 2.0
	9	ESATA
	10	Express Card
	11	BT 4.0
	12	Carmera
	13	Touch Screen
USH	0	BIO
	1	NA

PCI EXPRESS	DESTINATION
Lane 1	MINI CARD-1 WWAN
Lane 2	MINI CARD-2 WLAN
Lane 3	Express Card
Lane 4	NA
Lane 5	MINI CARD-3 (Pink Panther)
Lane 6	NVRAM Card
Lane 7	10/100/1G LOM
Lane 8	Cardreader

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Index and Config.			
Title	LA-7933		
Size	Document Number	Rev	0.2
Date	Monday, November 07, 2011	Sheet	3 of 65

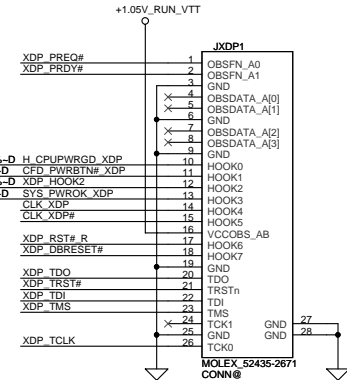
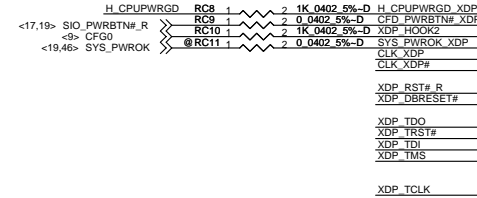
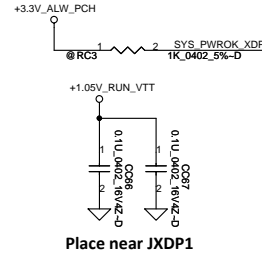
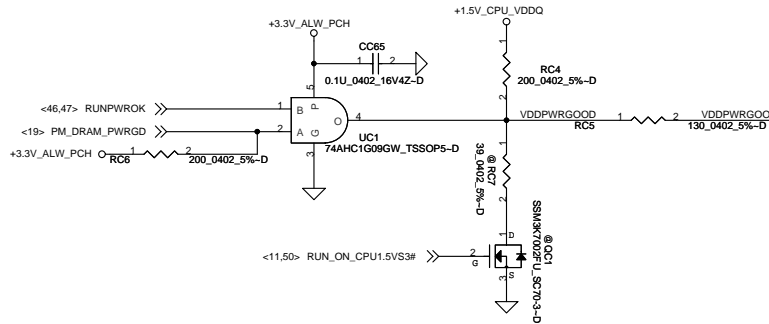
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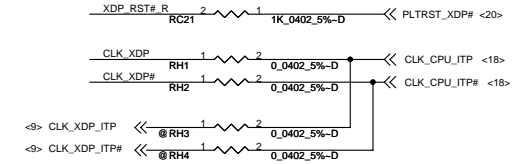
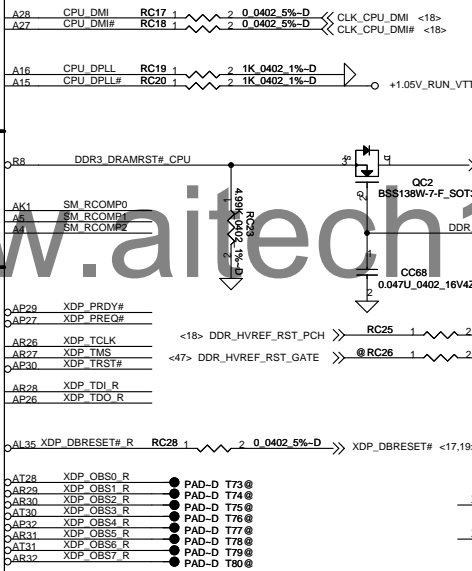
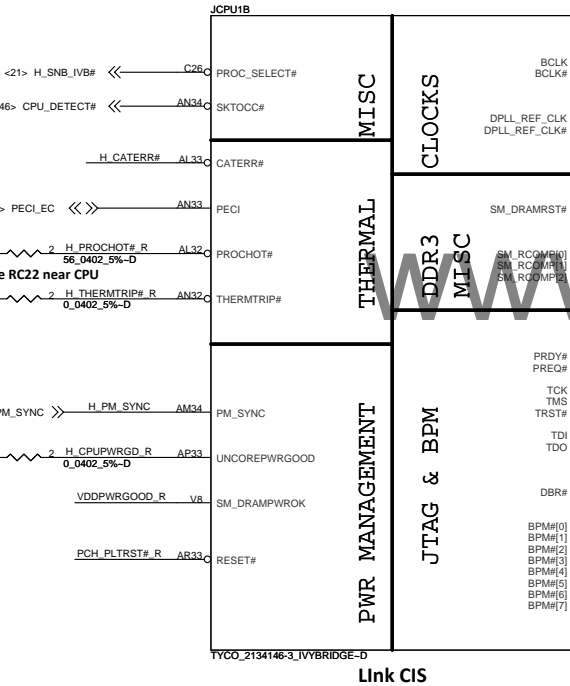
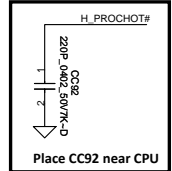




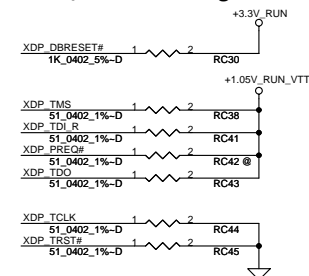
# Follow DG Rev0.71 SM\_DRAMPWROK topology



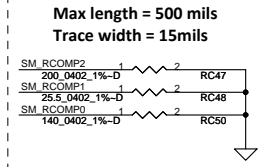
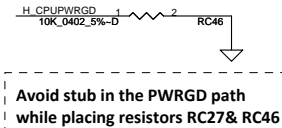
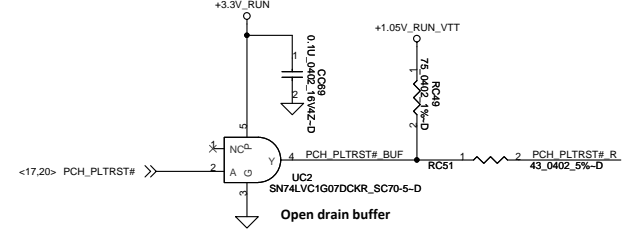
Avoid Power\_SRC trace noise coupling effect to CPU



## PU/PD for JTAG signals



## Buffered reset to CPU



Avoid stub in the PWRGD path while placing resistors RC27& RC46

Max length = 500 mils  
Trace width = 15mils

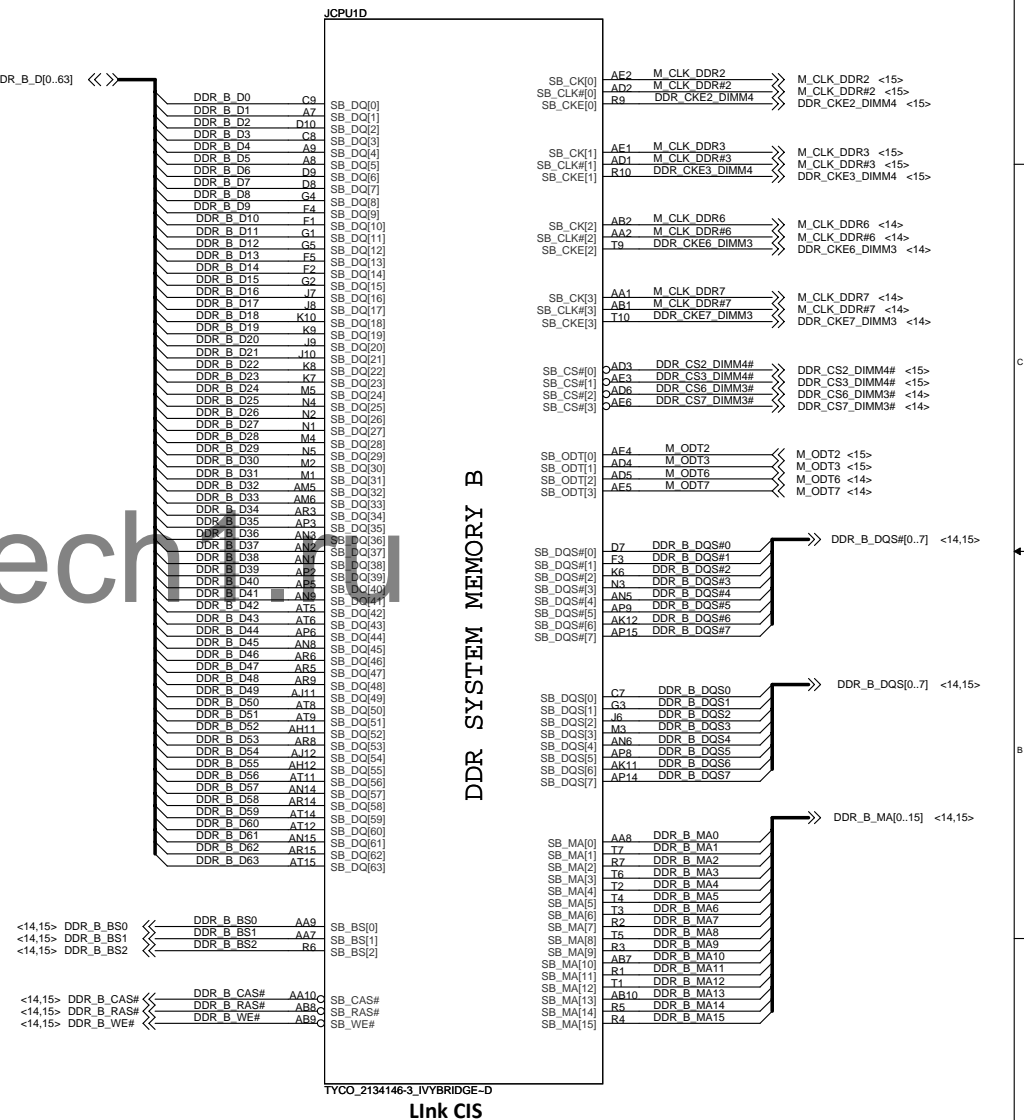
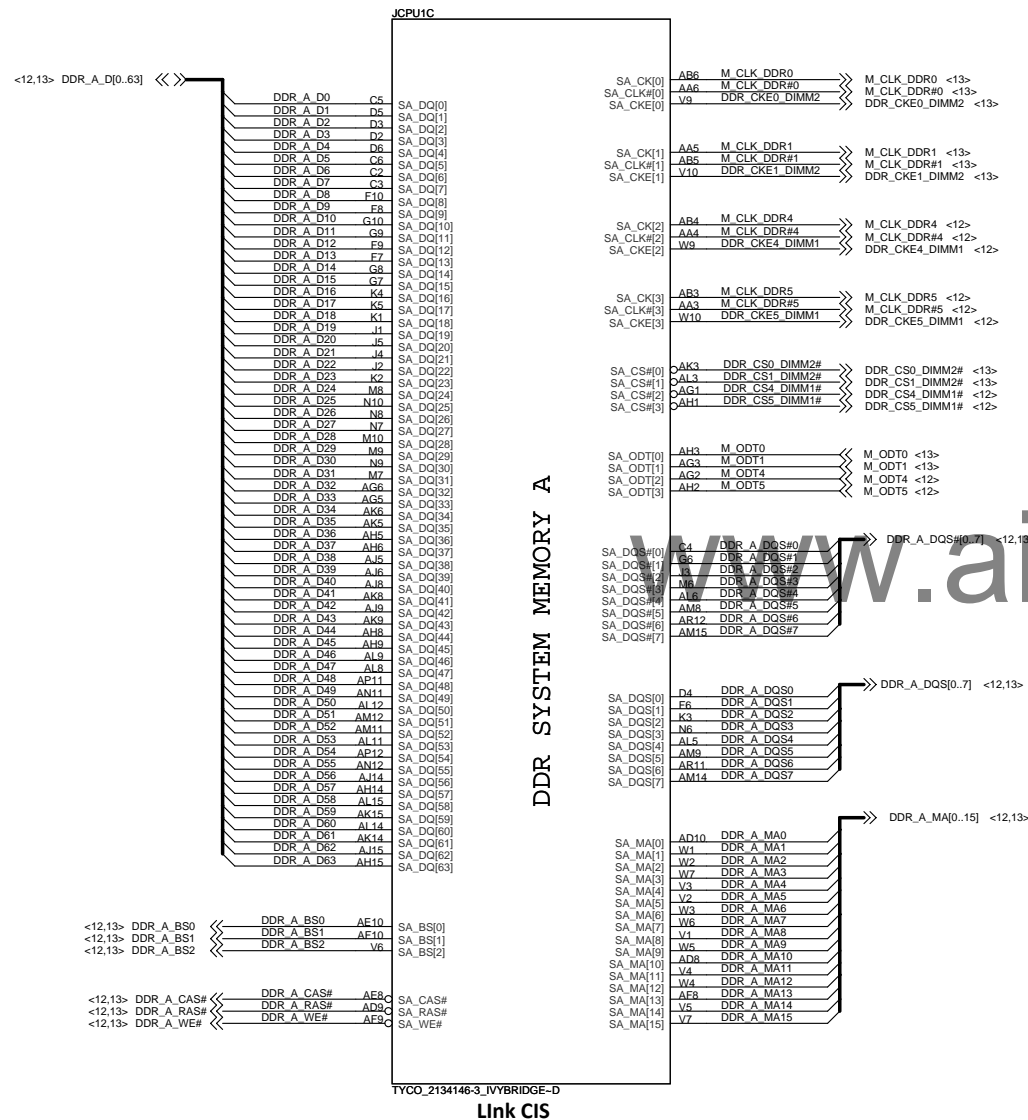
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Ivy Bridge (2/6)

File	Document Number	Rev
LA-7933	LA-7933	0.2
Date	Sheet	of
Tuesday, November 08, 2011	7	85

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Ivy Bridge (3/6)

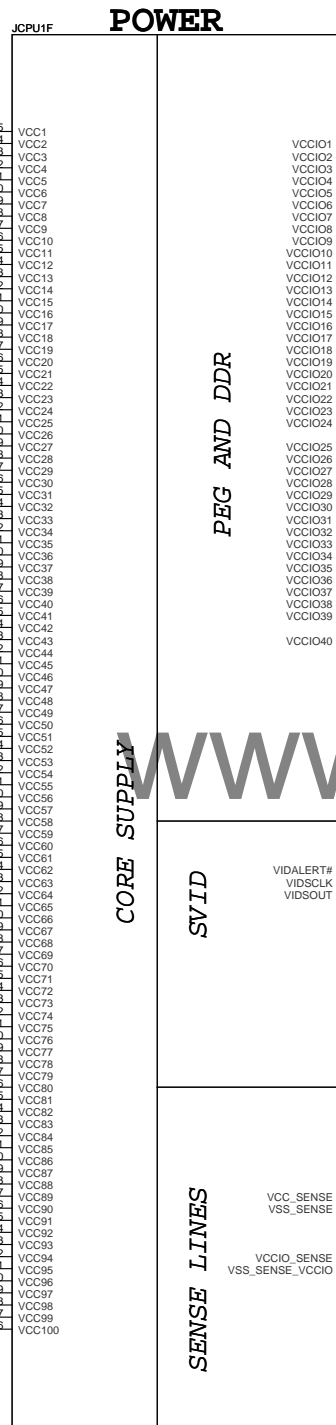
LA-7933

Title	Ivy Bridge (3/6)		
Size	Document Number	Rev 0.2	
Date	Monday, November 07, 2011	Sheet 8	of 65

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CORE SUPPLY

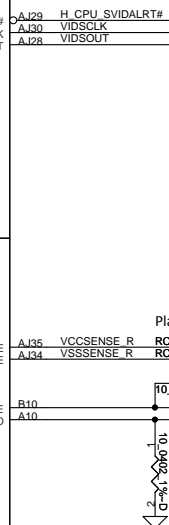
SVID

SENSE LINES

Link CIS

TYCO\_2134146-3\_IVYBRIDGE-D

VIDALERT#  
VIDCLK  
VIDSOUT  
VCC\_SENSE  
VSS\_SENSE  
VCCIO\_SENSE  
VSS\_SENSE\_VCCIO



Note: Place the PU resistors close to CPU  
RC63 close to CPU 300 - 1500mils

CAD Note: Place the PU resistors close to CPU  
RC65 close to CPU 300 - 1500mils

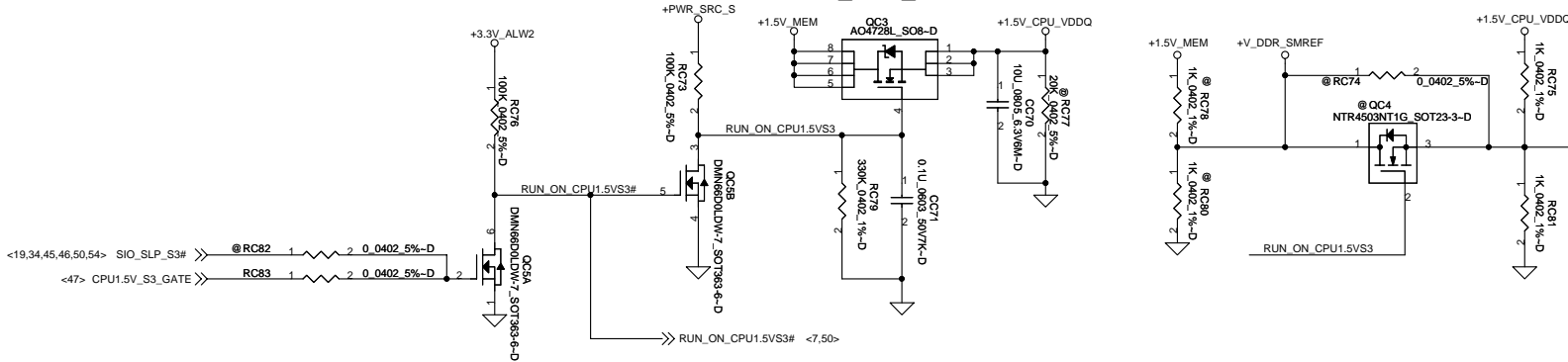
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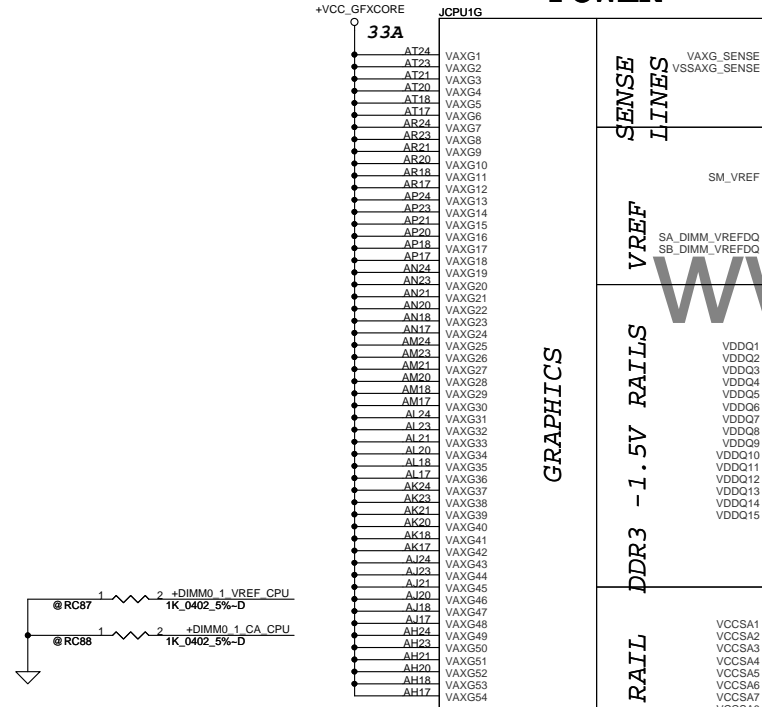


Title			
Ivy Bridge (5/6)			
Size	Document Number	Rev	
	LA-7933	0.2	
Date:	Monday, November 07, 2011	Sheet	10 of 65

# +1.5V\_CPU\_VDDQ Source



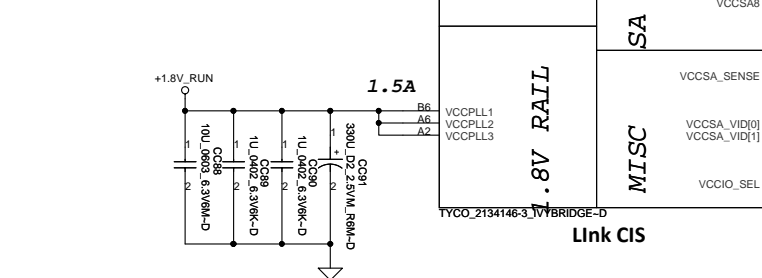
## POWER



## GRAPHICS

## SA RAIL DDR3 - 1.5V RAILS

## MISC



## Link CIS

JCPU1H		Link CIS	
AT35	VSS2	VSS81	AJ22
AT32	VSS2	VSS82	AJ19
AT29	VSS3	VSS83	AJ16
AT27	VSS4	VSS84	AJ13
AT25	VSS5	VSS85	AJ10
AT22	VSS6	VSS86	AJ7
AT19	VSS7	VSS87	AJ4
AT16	VSS8	VSS88	AJ3
AT13	VSS9	VSS89	AJ2
AT10	VSS10	VSS90	AJ1
AT7	VSS11	VSS91	AH35
AT4	VSS12	VSS92	AH34
AT3	VSS13	VSS93	AH32
AR25	VSS14	VSS94	AH30
AR22	VSS15	VSS95	AH29
AR19	VSS16	VSS96	AH28
AR16	VSS17	VSS97	AH25
AR13	VSS18	VSS98	AH22
AR10	VSS19	VSS99	AH19
AR7	VSS20	VSS100	AH16
AR4	VSS21	VSS101	AH12
AR2	VSS22	VSS102	AH7
AP34	VSS23	VSS103	AH4
AP31	VSS24	VSS104	AG9
AP28	VSS25	VSS105	AG8
AP25	VSS26	VSS106	AG4
AP22	VSS27	VSS107	AF8
AP19	VSS28	VSS108	AF5
AP16	VSS29	VSS109	AF3
AP13	VSS30	VSS110	AF2
AP10	VSS31	VSS111	AF35
AP7	VSS32	VSS112	AE34
AP4	VSS33	VSS113	AE33
AN30	VSS34	VSS114	AE32
AN27	VSS35	VSS115	AE31
AN25	VSS36	VSS116	AE30
AN22	VSS37	VSS117	AE29
AN19	VSS38	VSS118	AE28
AN16	VSS39	VSS119	AE27
AN13	VSS40	VSS120	AE26
AN10	VSS41	VSS121	AE25
AN7	VSS42	VSS122	AE24
AN4	VSS43	VSS123	AE23
AM29	VSS44	VSS124	AE22
AM25	VSS45	VSS125	AE21
AM22	VSS46	VSS126	AE20
AM19	VSS47	VSS127	AE19
AM16	VSS48	VSS128	AE18
AM13	VSS49	VSS129	AE17
AM10	VSS50	VSS130	AE16
AM7	VSS51	VSS131	AE15
AM4	VSS52	VSS132	AE14
AM3	VSS53	VSS133	AE13
AM2	VSS54	VSS134	AE12
AM1	VSS55	VSS135	AE11
AL34	VSS56	VSS136	AE10
AL31	VSS57	VSS137	AE9
AL28	VSS58	VSS138	AE8
AL25	VSS59	VSS139	AE7
AL22	VSS60	VSS140	AE6
AL19	VSS61	VSS141	AE5
AL16	VSS62	VSS142	AE4
AL13	VSS63	VSS143	AE3
AL10	VSS64	VSS144	AE2
AL7	VSS65	VSS145	AE1
AL4	VSS66	VSS146	W35
AK33	VSS67	VSS147	W34
AK30	VSS68	VSS148	W33
AK27	VSS69	VSS149	W32
AK25	VSS70	VSS150	W31
AK22	VSS71	VSS151	W30
AK19	VSS72	VSS152	W29
AK16	VSS73	VSS153	W28
AK13	VSS74	VSS154	W27
AK10	VSS75	VSS155	W26
AK7	VSS76	VSS156	W25
AK4	VSS77	VSS157	W24
AI25	VSS78	VSS158	W23
	VSS79	VSS159	W22
	VSS80	VSS160	W21

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## Ivy Bridge (6/6)

## LA-7933

## Rev 0.2

## Date: Monday, November 07, 2011 Sheet 11 of 65

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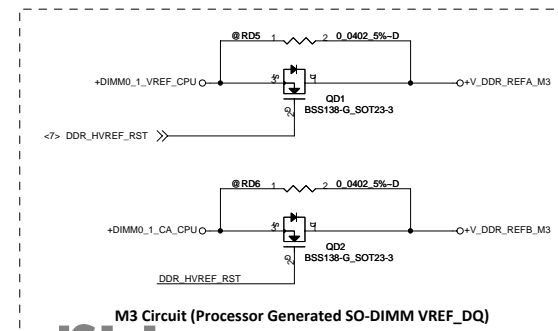
Populate RD1, De-Populate RD2 for Intel DDR3  
VREFDQ multiple methods M1  
Populate RD2, De-Populate RD1 for Intel DDR3  
VREFDQ multiple methods M3

	SA0	SA1
DIMM2	0	0
DIMM4	0	1
DIMM1	1	0
DIMM3	1	1

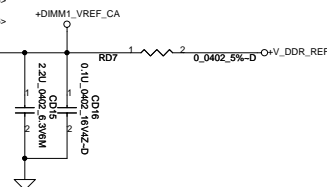
0.1u\_0402\_16V4Z-D

Diagram illustrating the memory layout for the top and bottom sides of the board:

- Top Side:** CPU, JDIMM1, JDIMM3
- Bottom Side:** JDIMM2, JDIMM4

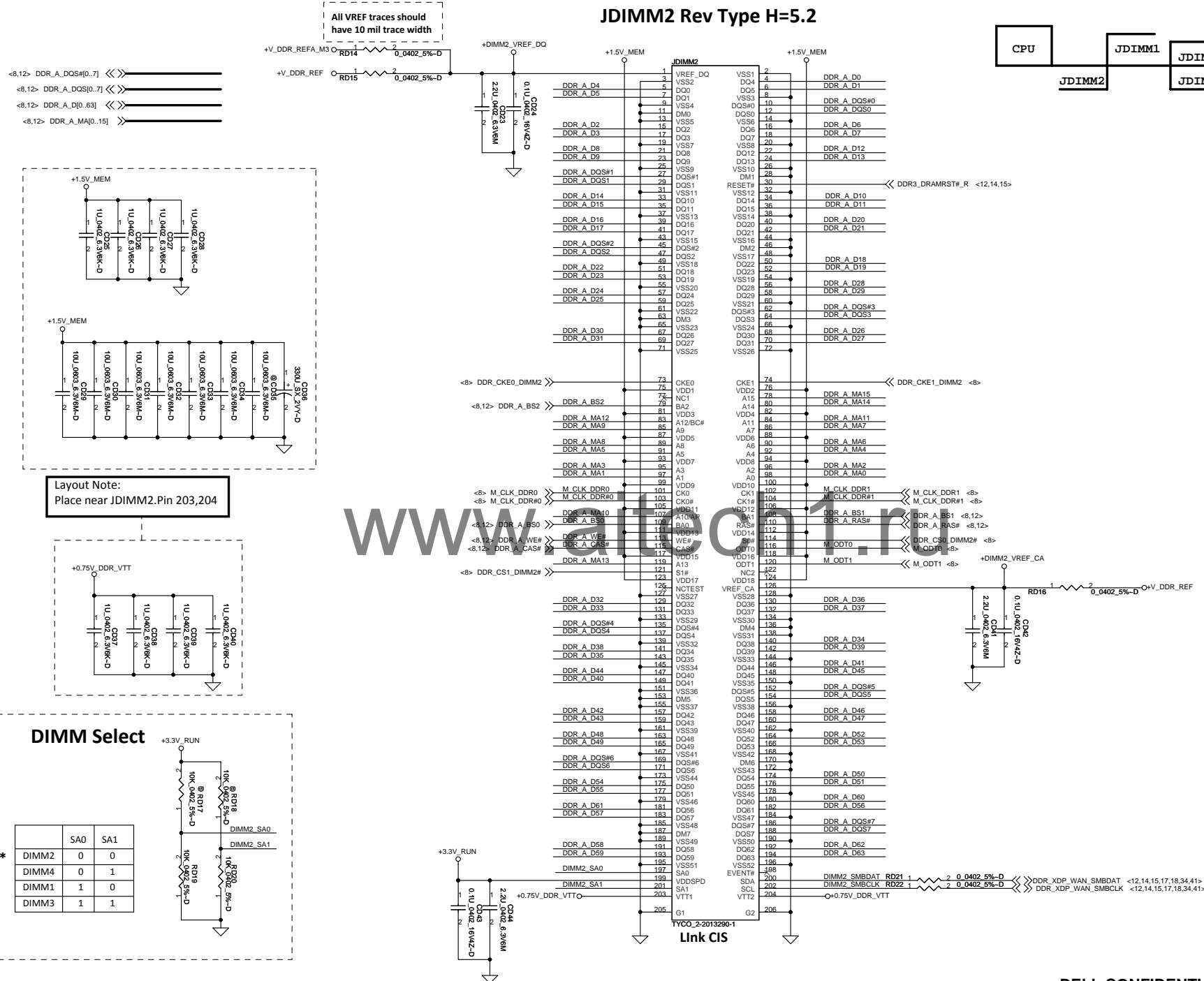
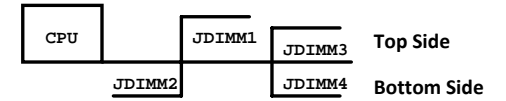


### M3 Circuit (Processor Generated SO-DIMM VREF\_DQ)



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# JDIMM2 Rev Type H=5.2



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DDR3-SODIMM SLOT2

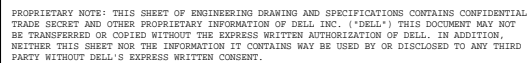
LA-7933

Date: Monday, November 07, 2011 Sheet: 13 of 85

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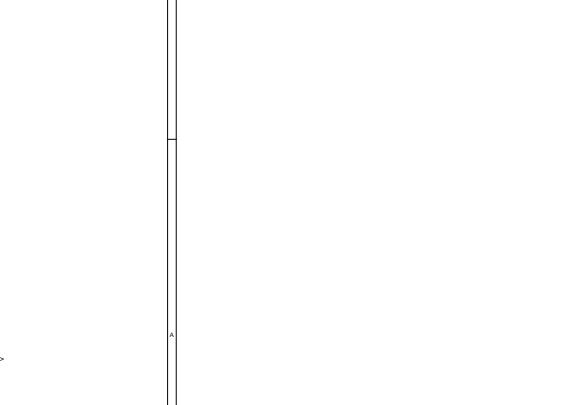
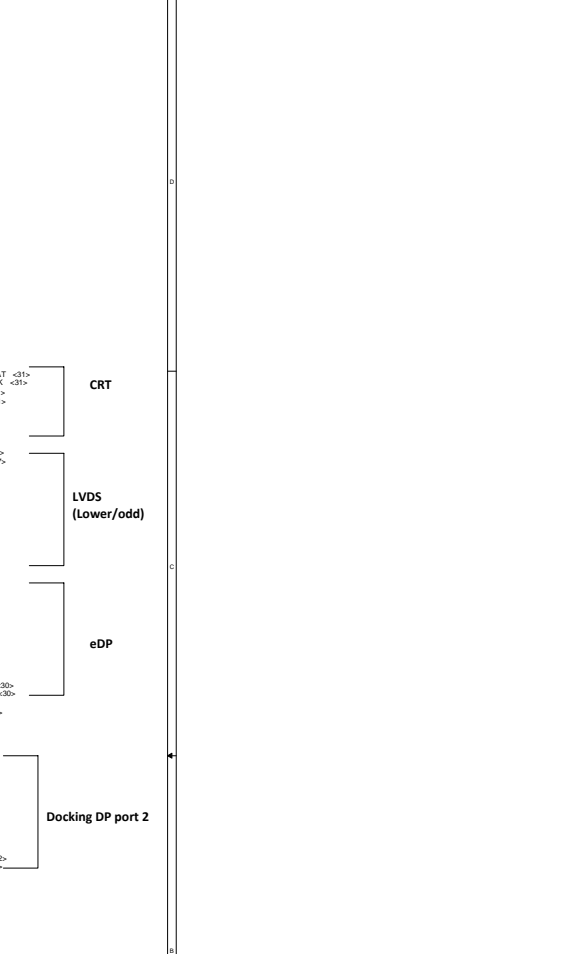
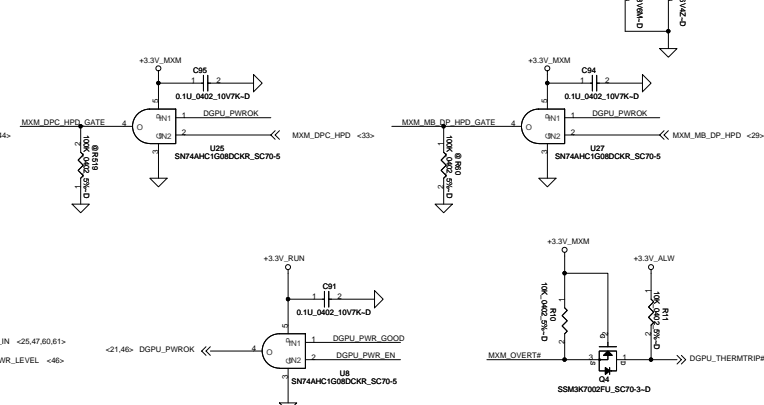
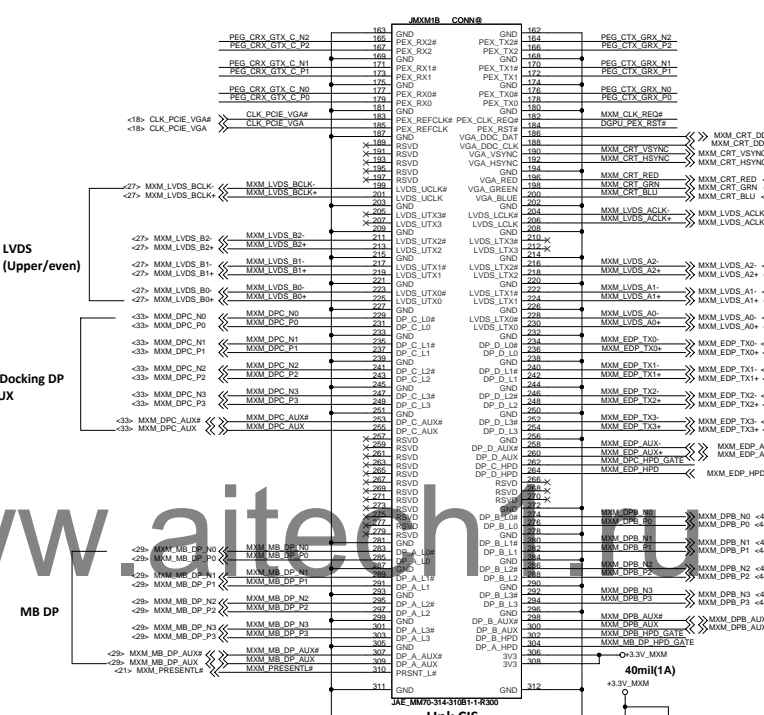
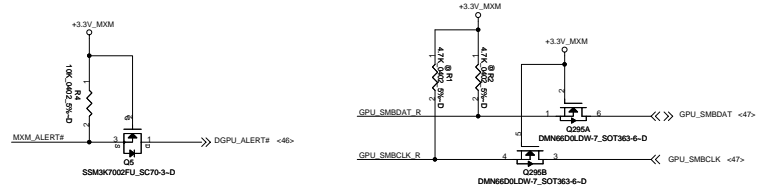
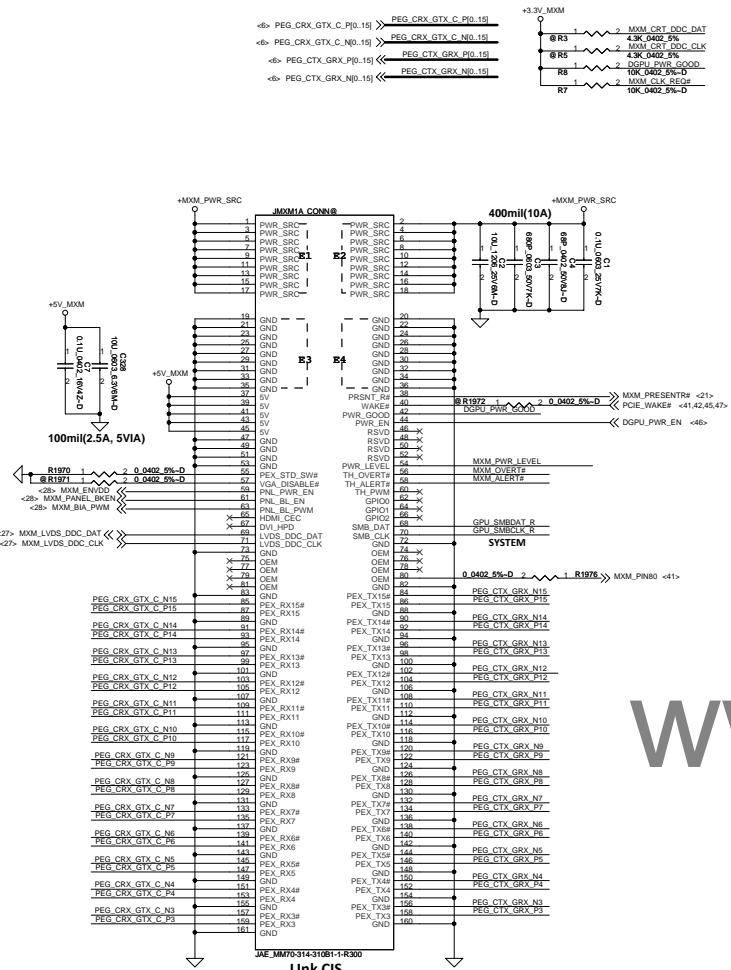
Diagram illustrating the top and bottom sides of the CPU module:

- Top Side:** CPU, JDIMM1, JDIMM3
- Bottom Side:** JDIMM2, JDIMM4



Size	Document Number	Rev
	<b>LA-7933</b>	0.2
Date:	Monday, November 07, 2011	Sheet 14 of 65

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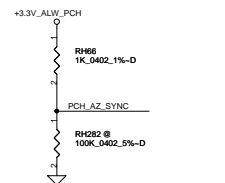
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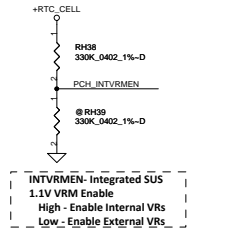
File	Document Number	Rev
MXM	LA-7933	0.2
Date:	Monday, November 07, 2011	Sheet 15 of 85

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PCH\_AZ\_SYNC is sampled at the rising edge of RSMRST# pin. So signal should be PU to the ALWAYS rail.

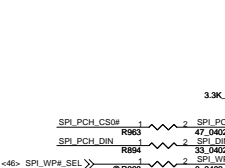
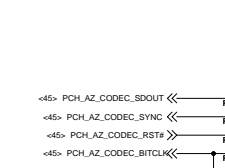


INTVRMEN-Integrated SUS 1.1V VRM Enable  
High - Enable Internal VRs  
Low - Enable External VRs



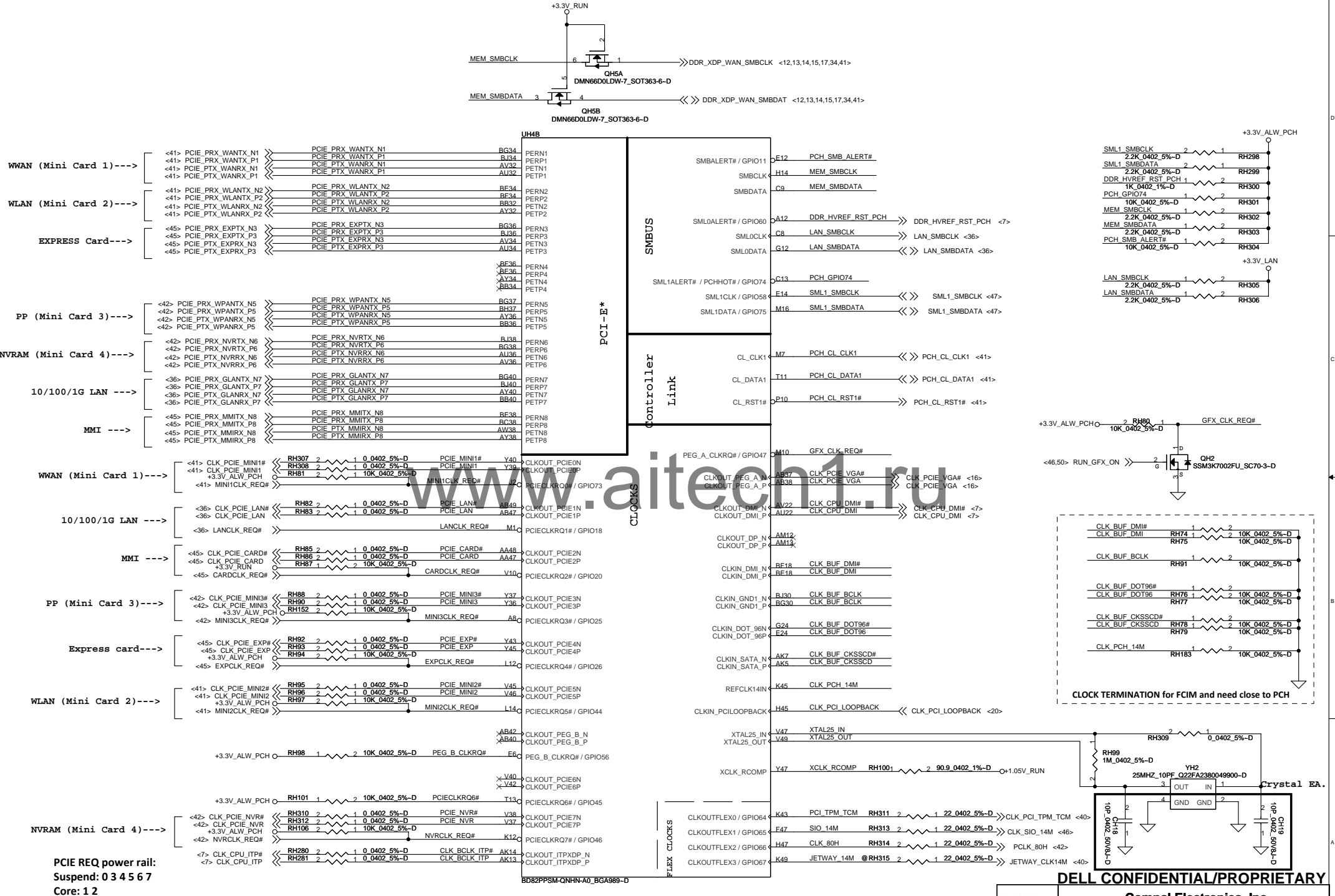
CMOS_CLR1	CMOS setting
Shunt	Clear CMOS
Open	Keep CMOS

ME_CLR1	TPM setting
Shunt	Clear ME RTC Registers
Open	Keep ME RTC Registers

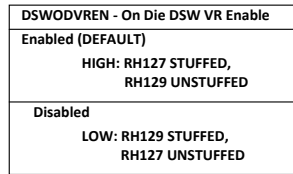


Pin	Signal	Value
20	USB_OC1W_R	33.0402_1%-D
21	USB_OC1W_R	33.0402_1%-D
22	USB_OC2W_R	33.0402_1%-D
23	USB_OC2W_R	33.0402_1%-D
24	USB_OC3W_R	33.0402_1%-D
25	USB_OC3W_R	33.0402_1%-D
26	USB_OC4W_R	33.0402_1%-D
27	USB_OC4W_R	33.0402_1%-D
28	USB_OC5W_R	33.0402_1%-D
29	USB_OC5W_R	33.0402_1%-D
30	USB_OC6W_R	33.0402_1%-D
31	USB_OC6W_R	33.0402_1%-D
32	USB_OC7W_R	33.0402_1%-D
33	USB_OC7W_R	33.0402_1%-D
34	USB_OC8W_R	33.0402_1%-D
35	USB_OC8W_R	33.0402_1%-D
36	USB_OC9W_R	33.0402_1%-D
37	USB_OC9W_R	33.0402_1%-D
38	USB_OC10W_R	33.0402_1%-D
39	USB_OC10W_R	33.0402_1%-D
40	USB_OC11W_R	33.0402_1%-D
41	USB_OC11W_R	33.0402_1%-D
42	USB_OC12W_R	33.0402_1%-D
43	USB_OC12W_R	33.0402_1%-D
44	USB_OC13W_R	33.0402_1%-D
45	USB_OC13W_R	33.0402_1%-D
46	USB_OC14W_R	33.0402_1%-D
47	USB_OC14W_R	33.0402_1%-D
48	USB_OC15W_R	33.0402_1%-D
49	USB_OC15W_R	33.0402_1%-D
50	USB_OC16W_R	33.0402_1%-D
51	USB_OC16W_R	33.0402_1%-D
52	USB_OC17W_R	33.0402_1%-D
53	USB_OC17W_R	33.0402_1%-D
54	USB_OC18W_R	33.0402_1%-D
55	USB_OC18W_R	33.0402_1%-D
56	USB_OC19W_R	33.0402_1%-D
57	USB_OC19W_R	33.0402_1%-D
58	USB_OC20W_R	33.0402_1%-D
59	USB_OC20W_R	33.0402_1%-D
60	USB_OC21W_R	33.0402_1%-D
61	USB_OC21W_R	33.0402_1%-D
62	USB_OC22W_R	33.0402_1%-D
63	USB_OC22W_R	33.0402_1%-D
64	USB_OC23W_R	33.0402_1%-D
65	USB_OC23W_R	33.0402_1%-D
66	USB_OC24W_R	33.0402_1%-D
67	USB_OC24W_R	33.0402_1%-D
68	USB_OC25W_R	33.0402_1%-D
69	USB_OC25W_R	33.0402_1%-D
70	USB_OC26W_R	33.0402_1%-D
71	USB_OC26W_R	33.0402_1%-D
72	USB_OC27W_R	33.0402_1%-D
73	USB_OC27W_R	33.0402_1%-D
74	USB_OC28W_R	33.0402_1%-D
75	USB_OC28W_R	33.0402_1%-D
76	USB_OC29W_R	33.0402_1%-D
77	USB_OC29W_R	33.0402_1%-D
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79	USB_OC30W_R	33.0402_1%-D
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81	USB_OC31W_R	33.0402_1%-D
82	USB_OC32W_R	33.0402_1%-D
83	USB_OC32W_R	33.0402_1%-D
84	USB_OC33W_R	33.0402_1%-D
85	USB_OC33W_R	33.0402_1%-D
86	USB_OC34W_R	33.0402_1%-D
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91	USB_OC36W_R	33.0402_1%-D
92	USB_OC37W_R	33.0402_1%-D
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95	USB_OC38W_R	33.0402_1%-D
96	USB_OC39W_R	33.0402_1%-D
97	USB_OC39W_R	33.0402_1%-D
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107	USB_OC44W_R	33.0402_1%-D
108	USB_OC45W_R	33.0402_1%-D
109	USB_OC45W_R	33.0402_1%-D
110	USB_OC46W_R	33.0402_1%-D
111	USB_OC46W_R	33.0402_1%-D
112	USB_OC47W_R	33.0402_1%-D
113	USB_OC47W_R	33.0402_1%-D
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118	USB_OC50W_R	33.0402_1%-D
119	USB_OC50W_R	33.0402_1%-D
120	USB_OC51W_R	33.0402_1%-D
121	USB_OC51W_R	33.0402_1%-D
122	USB_OC52W_R	33.0402_1%-D
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136	USB_OC59W_R	33.0402_1%-D
137	USB_OC59W_R	33.0402_1%-D
138	USB_OC60W_R	33.0402_1%-D
139	USB_OC60W_R	33.0402_1%-D
140	USB_OC61W_R	33.0402_1%-D
141	USB_OC61W_R	33.0402_1%-D
142	USB_OC62W_R	33.0402_1%-D
143	USB_OC62W_R	33.0402_1%-D
144	USB_OC63W_R	33.0402_1%-D
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147	USB_OC64W_R	33.0402_1%-D
148	USB_OC65W_R	33.0402_1%-D
149	USB_OC65W_R	33.0402_1%-D
150	USB_OC66W_R	33.0402_1%-D
151	USB_OC66W_R	33.0402_1%-D
152	USB_OC67W_R	33.0402_1%-D
153	USB_OC67W_R	33.0402_1%-D
154	USB_OC68W_R	33.0402_1%-D
155	USB_OC68W_R	33.0402_1%-D
156	USB_OC69W_R	33.0402_1%-D
157	USB_OC69W_R	33.0402_1%-D
158	USB_OC70W_R	33.0402_1%-D
159	USB_OC70W_R	33.0402_1%-D
160	USB_OC71W_R	33.0402_1%-D
161	USB_OC71W_R	33.0402_1%-D
162	USB_OC72W_R	33.0402_1%-D
163	USB_OC72W_R	33.0402_1%-D
164	USB_OC73W_R	33.0402_1%-D
165	USB_OC73W_R	33.0402_1%-D
166	USB_OC74W_R	33.0402_1%-D
167	USB_OC74W_R	33.0402_1%-D
168	USB_OC75W_R	33.0402_1%-D
169	USB_OC75W_R	33.0402_1%-D
170	USB_OC76W_R	33.0402_1%-D
171	USB_OC76W_R	33.0402_1%-D
172	USB_OC77W_R	33.0402_1%-D
173	USB_OC77W_R	33.0402_1%-D
174	USB_OC78W_R	33.0402_1%-D
175	USB_OC78W_R	33.0402_1%-D
176	USB_OC79W_R	33.0402_1%-D
177	USB_OC79W_R	33.0402_1%-D
178	USB_OC80W_R	33.0402_1%-D
179	USB_OC80W_R	33.0402_1%-D
180	USB_OC81W_R	33.0402_1%-D
181	USB_OC81W_R	33.0402_1%-D
182	USB_OC82W_R	33.0402_1%-D
183	USB_OC82W_R	33.0402_1%-D
184	USB_OC83W_R	33.0402_1%-D
185	USB_OC83W_R	33.0402_1%-D
186	USB_OC84W_R	33.0402_1%-D
187	USB_OC84W_R	33.0402_1%-D
188	USB_OC85W_R	33.0402_1%-D
189	USB_OC85W_R	33.0402_1%-D
190	USB_OC86W_R	33.0402_1%-D
191	USB_OC86W_R	33.0402_1%-D
192	USB_OC87W_R	33.0402_1%-D
193	USB_OC87W_R	33.0402_1%-D
194	USB_OC88W_R	33.0402_1%-D
195	USB_OC88W_R	33.0402_1%-D
196	USB_OC89W_R	33.0402_1%-D
197	USB_OC89W_R	33.0402_1%-D
198	USB_OC90W_R	33.0402_1%-D
199	USB_OC90W_R	33.0402_1%-D
200	USB_OC91W_R	33.0402_1%-D
201	USB_OC91W_R	33.0402_1%-D
202	USB_OC92W_R	33.0402_1%-D
203	USB_OC92W_R	33.0402_1%-D
204	USB_OC93W_R	33.0402_1%-D
205	USB_OC93W_R	33.0402_1%-D
206	USB_OC94W_R	33.0402_1%-D
207	USB_OC94W_R	33.0402_1%-D
208	USB_OC95W_R	33.0402_1%-D
209	USB_OC95W_R	33.0402_1%-D
210	USB_OC96W_R	33.0402_1%-D
211	USB_OC96W_R	33.0402_1%-D
212	USB_OC97W_R	33.0402_1%-D
213	USB_OC97W_R	33.0402_1%-D
214	USB_OC98W_R	33.0402_1%-D
215	USB_OC98W_R	33.0402_1%-D
216	USB_OC99W_R	33.0402_1%-D
217	USB_OC99W_R	33.0402_1%-D
218	USB_OC100W_R	33.0402_1%-D
219	USB_OC100W_R	33.0402_1%-D

Pin	Signal	Value
21	USB_OC1W_R	33.0402_1%-D
22	USB_OC2W_R	33.0402_1%-D
23	USB_OC3W_R	33.0402_1%-D
24	USB_OC4W_R	33.0402_1%-D
25	USB_OC5W_R	33.0402_1%-D
26	USB_OC6W_R	33.0402_1%-D
27	USB_OC7W_R	33.0402_1%-D
28	USB_OC8W_R	33.0402_1%-D
29	USB_OC9W_R	33.0402_1%-D
30	USB_OC10W_R	33.0402_1%-D
31	USB_OC11W_R	33.0402_1%-D
32	USB_OC12W_R	33.0402_1%-D
33	USB_OC13W_R	33.0402_1%-D
34	USB_OC14W_R	33.0402_1%-D
35	USB_OC15W_R	33.0402_1%-D
36	USB_OC16W_R	33.0402_1%-D
37	USB_OC17W_R	33.0402_1%-D
38	USB_OC18W_R	33.0402_1%-D
39	USB_OC19W_R	33.0402_1%-D
40	USB_OC20W_R	33.0402_1%-D
41	USB_OC21W_R	33.0402_1%-D
42	USB_OC22W_R	33.0402_1%-D
43	USB_OC23W_R	33.0402_1%-D
44	USB_OC24W_R	33.0402_1%-D
45	USB_OC25W_R	33.0402_1%-D
46	USB_OC26W_R	33.0402_1%-D
47	USB_OC27W_R	33.0402_1%-D
48	USB_OC28W_R	33.0402_1%-D
49	USB_OC29W_R	33.0402_1%-D
50	USB_OC30W_R	33.0402_1%-D
51	USB_OC31W_R	33.0402_1%-D
52	USB_OC32W_R	33.0402_1%-D
53	USB_OC33W_R	33.0402_1%-D
54	USB_OC34W_R	33.0402_1%-D
55	USB_OC35W_R	33.0402_1%-D
56	USB_OC36W_R	33.0402_1%-D
57	USB_OC37W_R	33.0402_1%-D
58	USB_OC38W_R	33.0402_1%-D
59	USB_OC39W_R	33.0402_1%-D
60	USB_OC40W_R	33.0402_1%-D
61	USB_OC41W_R	33.0402_1%-D
62	USB_OC42W_R	33.0402_1%-D
63	USB_OC43W_R	33.0402_1%-D
64	USB_OC44W_R	33.0402_1%-D
65	USB_OC45W_R	33.0402_1%-D
66	USB_OC46W_R	33.0402_1%-D
67	USB_OC47W_R	33.0402_1%-D
68	USB_OC48W_R	33.0402_1%-D
69	USB_OC49W_R	33.0402_1%-D
70	USB_OC50W_R	33.0402_1%-D
71	USB_OC51W_R	33.0402_1%-D
72	USB_OC52W_R	33.0402_1%-D
73	USB_OC53W_R	33.0402_1%-D
74	USB_OC54W_R	33.0402_1%-D
75	USB_OC55W_R	33.0402_1%-D
76	USB_OC56W_R	33.0402_1%-D
77	USB_OC57W_R	33.0402_1%-D
78	USB_OC58W_R	33.0402_1%-D
79	USB_OC59W_R	33.0402_1%-D
80	USB_OC60W_R	33.0402_1%-D
81	USB_OC61W_R	33.0402_1%-D
82	USB_OC62W_R	33.0402_1%-D
83	USB_OC63W_R	33.0402_1%-D
84	USB_OC64W_R	33.0402_1%-D
85	USB_OC65W_R	33.0402_1%-D
86	USB_OC66W_R	33.0402_1%-D
87	USB_OC67W_R	33.0402_1%-D
88	USB_OC68W_R	33.0402_1%-D
89	USB_OC69W_R	33.0402_1%-D
90	USB_OC70W_R	33.0402_1%-D
91	USB_OC71W_R	33.0402_1%-D
92	USB_OC72W_R	33.0402_1%-D
93	USB_OC73W_R	33.0402_1%-D
94	USB_OC74W_R	33.0402_1%-D
95	USB_OC75W_R	33.0402_1%-D
96	USB_OC76W_R	33.0402_1%-D
97	USB_OC77W_R	33.0402_1%-D
98	USB_OC78W_R	33.0402_1%-D
99	USB_OC79W_R	33.0402_1%-D
100	USB_OC80W_R	33.0402_1%-D
101	USB_OC81W_R	33.0402_1%-D
102	USB_OC82W_R	33.0402_1%-D
103	USB_OC83W_R	33.0402_1%-D
104	USB_OC84W_R	33.0402_1%-D
105	USB_OC85W_R	33.0402_1%-D
106	USB_OC86W_R	33.0402_1%-D
107	USB_OC87W_R	33.0402_1%-D

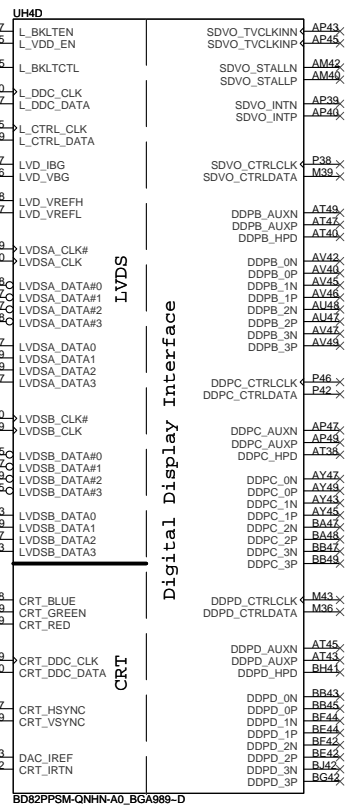
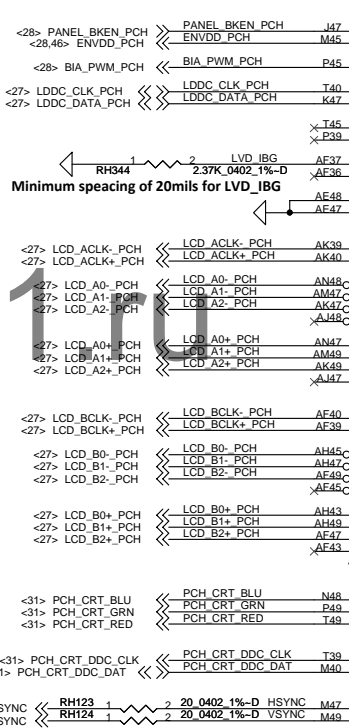


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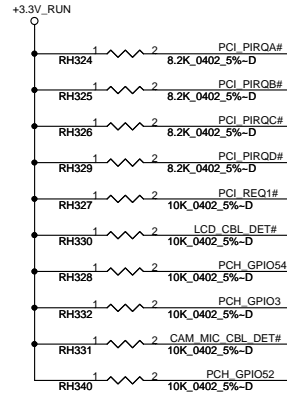


PCH\_CRT\_DDC\_CLK 2 1 RH317 @  
2.2K\_0402\_5%-D

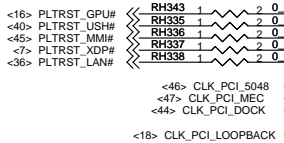
PCH\_CRT\_DDC\_DAT 1 2 RH316 @  
2.2K\_0402\_5%-D

**LA-7933**

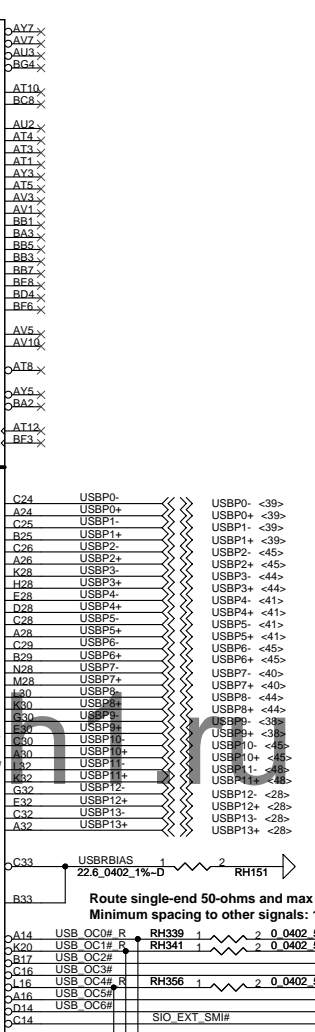
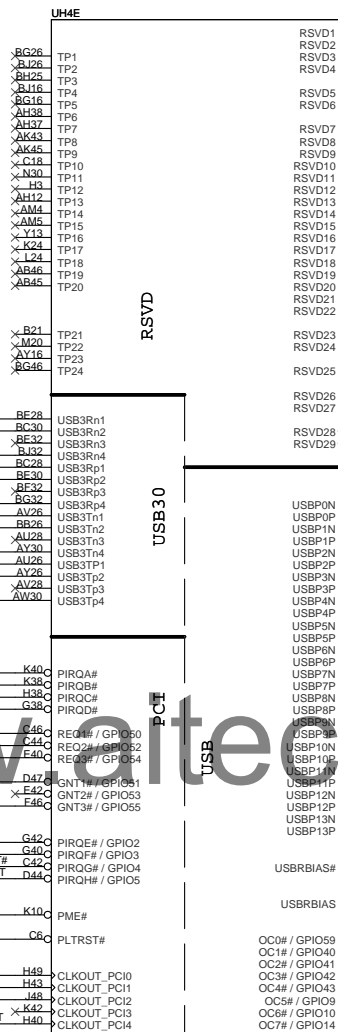
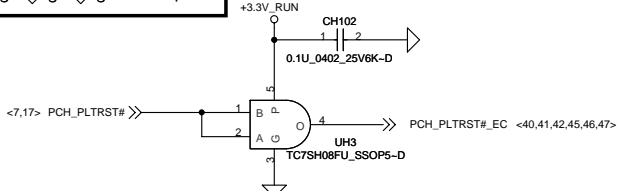
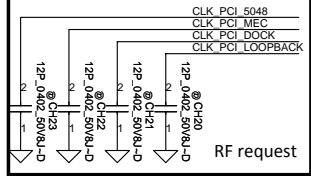
Date: Monday, November 07, 2011 Sheet 19 of 65



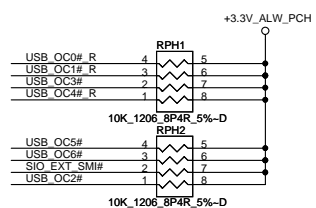
A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = A16 swap High = Default



Avoid WWAN noise affect PCI 3.3M CLK.

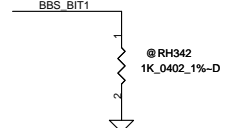


- >Right Side
- >Right Side
- >Left Side
- >MLK DOCK
- >WLAN/WIMAX
- >WWAN/UWB
- >Left Side
- >USH
- >DOCK
- >ESATA
- >Express Card
- >Blue Tooth
- >Camera
- >LCD Touch



Route single-end 50-ohms and max 500-mils length.  
Minimum spacing to other signals: 15 mils

Boot BIOS Strap		
BBS_BIT1	SATA_SLDP (BBS_BIT0)	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI



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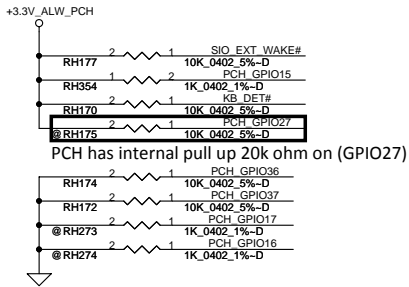
PCH (4/8)

LA-7933

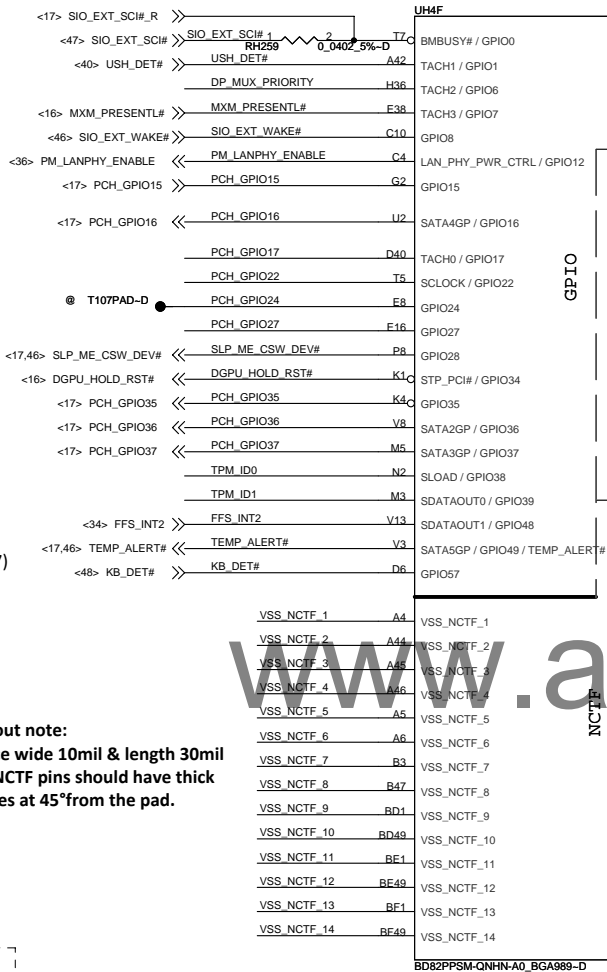
Size	Document Number	Rev
		0.2
Date:	Monday, November 07, 2011	Sheet 20 of 65

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SLP_ME_CSW_DEV# PLL ON DIE VR ENABLE	
ENABLED	HIGH (DEFAULT)
DISABLED	LOW

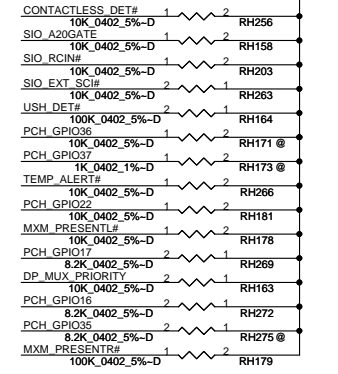


Layout note:  
Trace wide 10mil & length 30mil  
All NCTF pins should have thick traces at 45° from the pad.

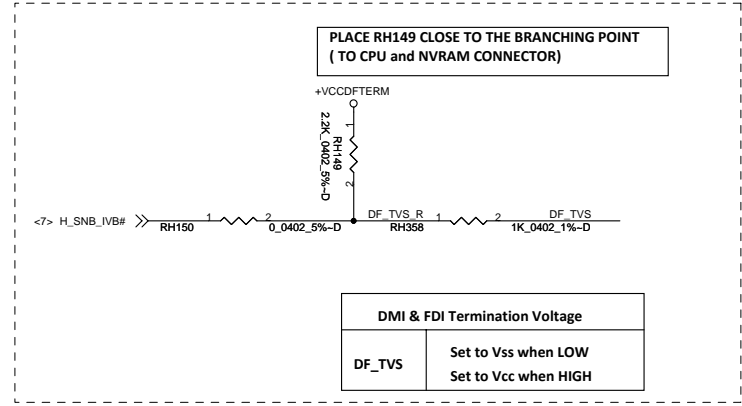


	TPM_ID0	TPM_ID1
China TPM	0	0
No TPM, No China TPM	0	1
TBD		
TPM	1	1

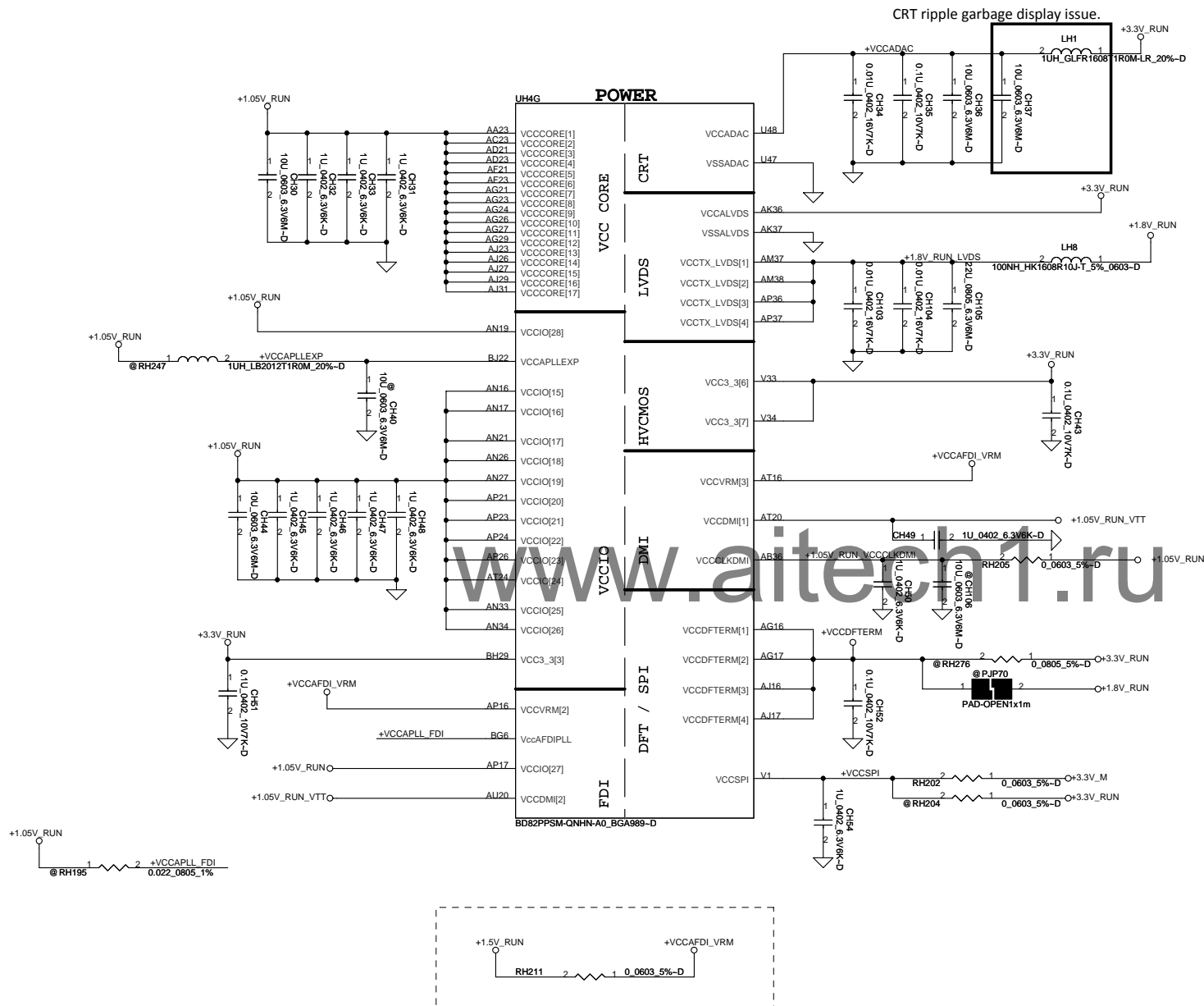
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Layout note:  
Trace wide 10mil & length 30mil  
All NCTF pins should have thick traces at 45° from the pad.



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Title			
PCH (5/8)			
Size	Document Number	Rev	
	LA-7933	0.2	
Date	Monday, November 07, 2011	Sheet	21 of 65



PCH Power Rail Table		
Voltage Rail	Voltage	S0 Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.228
VccADAC3	3.3	0.063
VccADPLLA	1.05	0.08
VccADPLLB	1.05	0.08
VccCore	1.05	1.7
VccDMI	1.1	0.047
VccIO	1.05	3.711
VccASW	1.05	0.903
VccSPI	3.3	0.01
VccDSW3_3	3.3	0.001
VCCDFTERM	1.8	0.002
VccRTC	3.3	2 (mA)
VccSus3_3	3.3	0.095
VccSusHDA	3.3	0.01
VccVRM	1.5	0.167
VccClkDMI	1.05	0.07
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.04

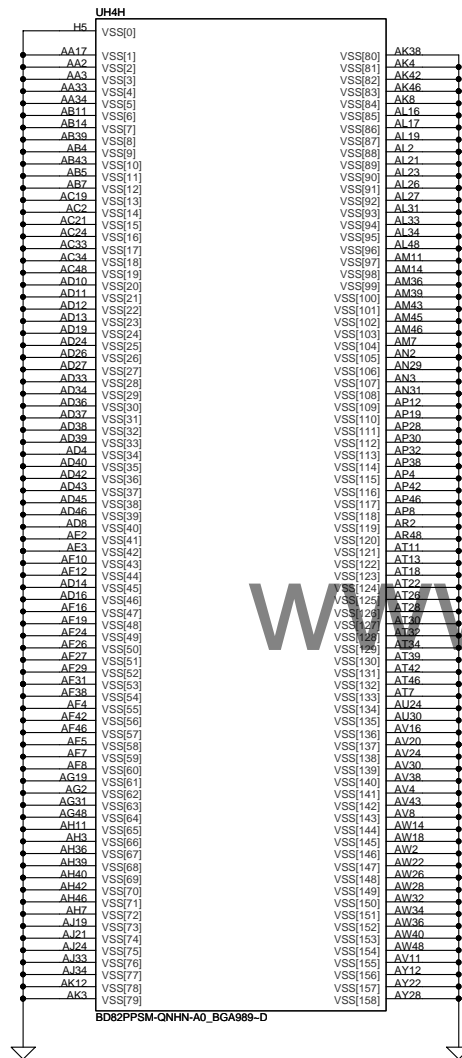
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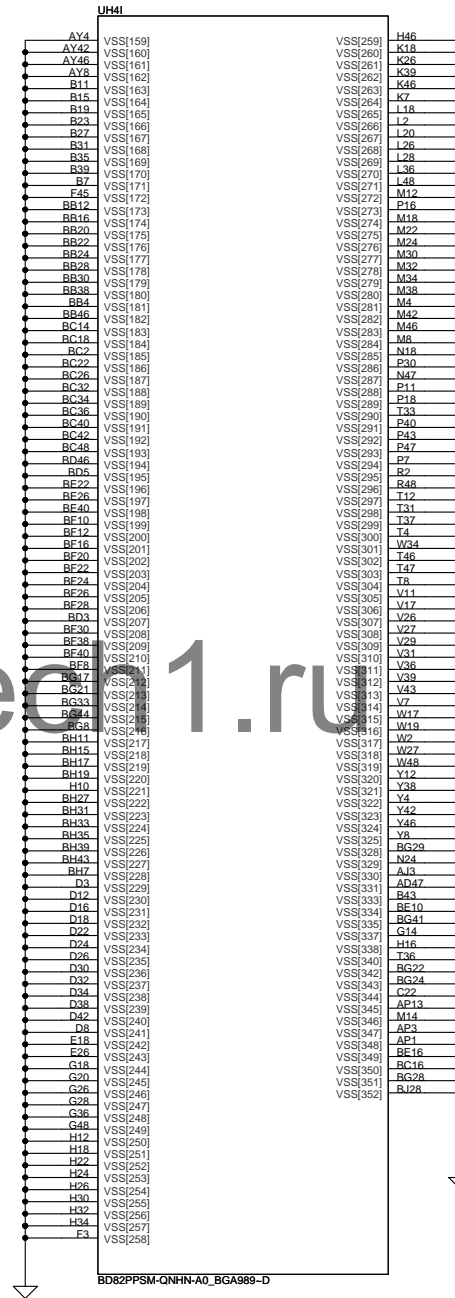
Title			PCH (6/8)
Size	Document Number	Rev	0.2
Date	Monday, November 07, 2011	Sheet	22 of 65

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BD82PPSM-QNHN-A0\_BGA989-D



BD82PPSM-QNHN-A0\_BGA989-D

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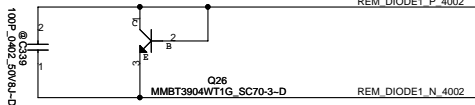
Compal Electronics, Inc.

Title <b>PCH (8/8)</b>		
Size	Document Number <b>LA-7933</b>	Rev <b>0.2</b>
Date	Monday, November 07, 2011	
Sheet	24	of 65

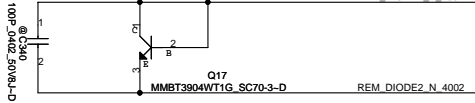
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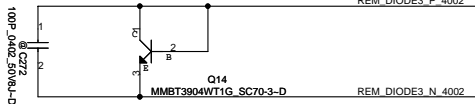
Place Q26 under CPU for OTP sensor.  
Place C266 close to the Q26 as possible



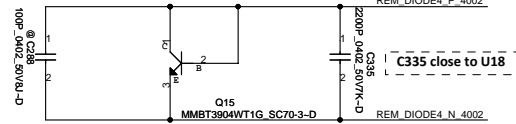
Put Q17 on the Bot side for Skin temperature



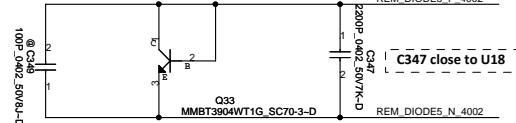
Place Q14 near Docking CONN on BOT side



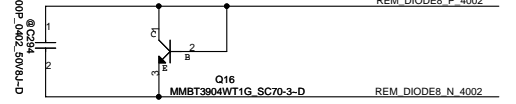
Place Q15 under Butterfly's CH A (BOT side).



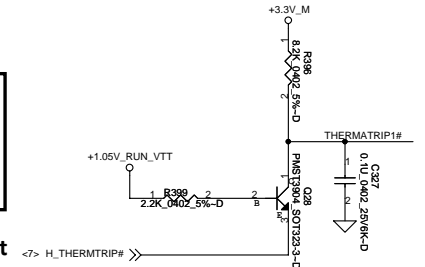
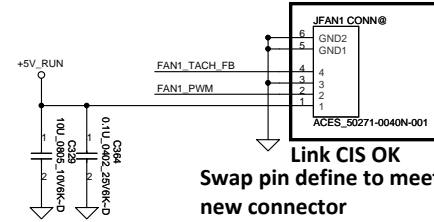
Place Q33 under Stack\_SODIMM on TOP side.



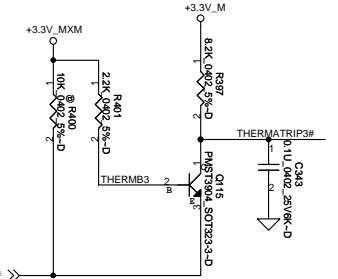
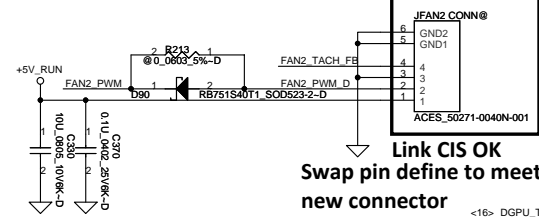
Place Q16 under Butterfly's CH B (BOT side).



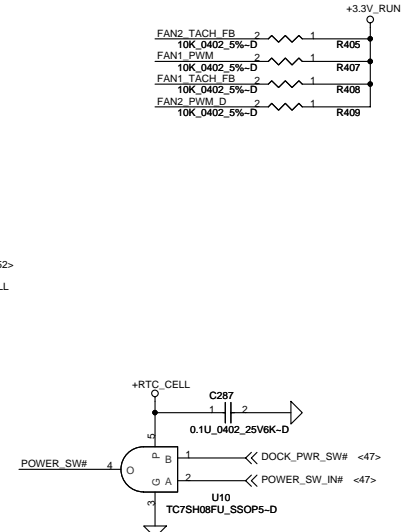
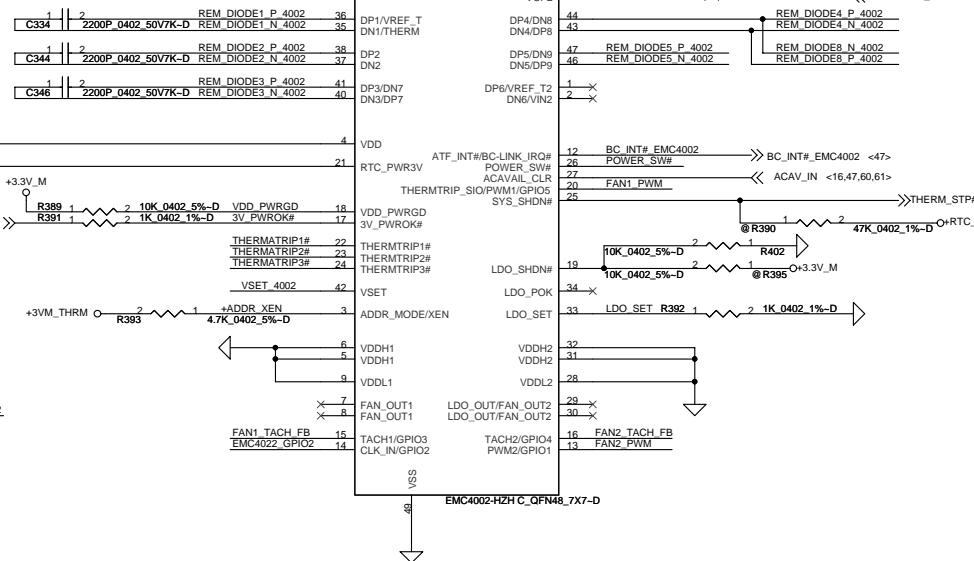
## CPU FAN



## MXM FAN



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FAN control

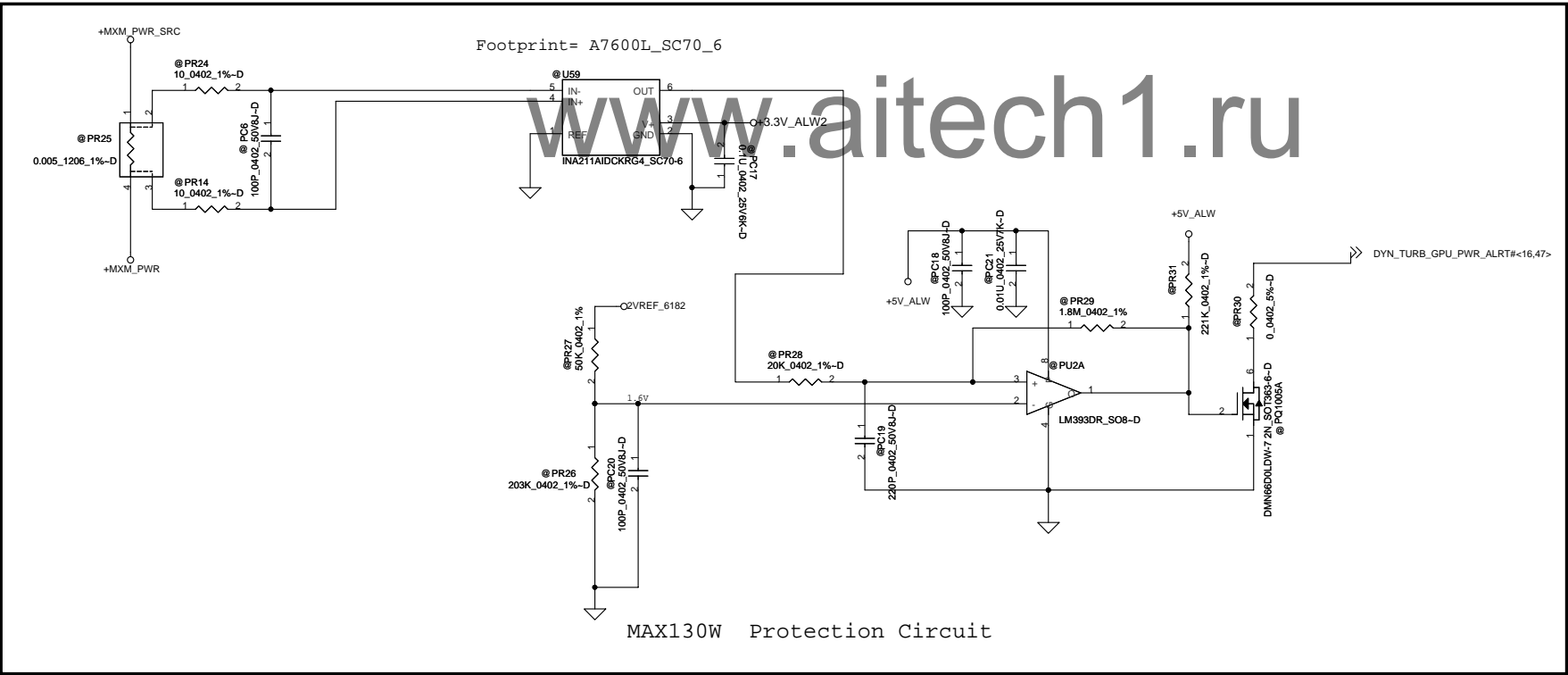
File	Document Number	Rev
LA-7933	0.2	
Date	Monday, November 07, 2011	Sheet 25 of 85

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# Monitor PWR\_SRC\_MXM

RESISTOR (5%)	SMBUS ADDRESS
0	1001_100(r/w)
100	1001_101(r/w)
180	1001_110(r/w)
300	1001_111(r/w)
430	1001_000(r/w)
560	1001_001(r/w)
750	1001_010(r/w)
1270	1001_011(r/w)
1600	0101_000(r/w)
2000	0101_001(r/w)
2700	0101_010(r/w)
3600	0101_011(r/w)
5600	0101_100(r/w)
9100	0101_100(r/w)
20000	0101_101(r/w)
Open	0011_000(r/w)

## Monitor PWR\_SRC\_MXM for DELL request



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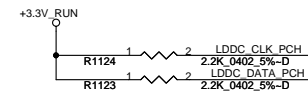
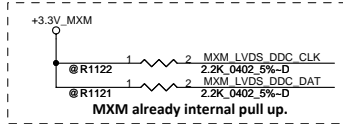
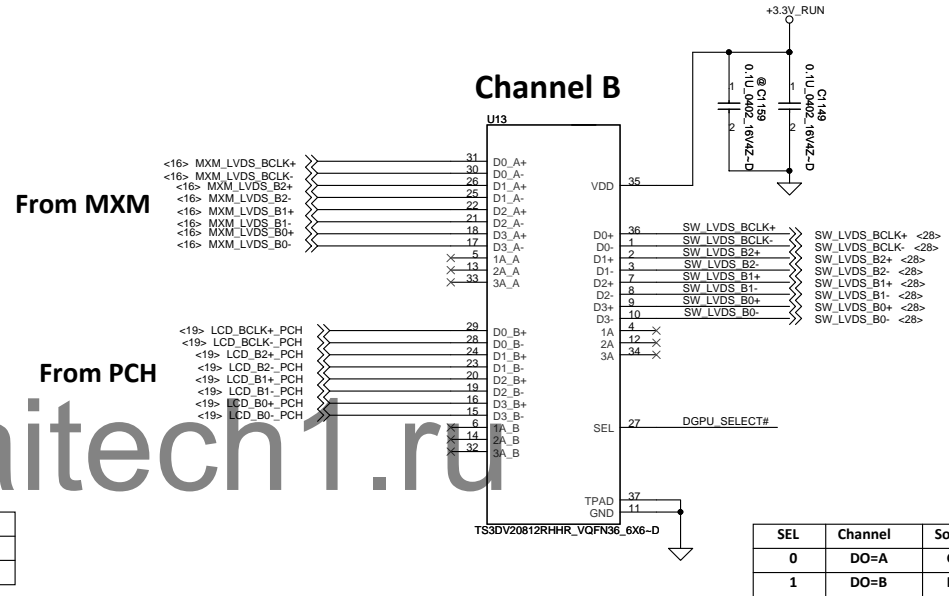
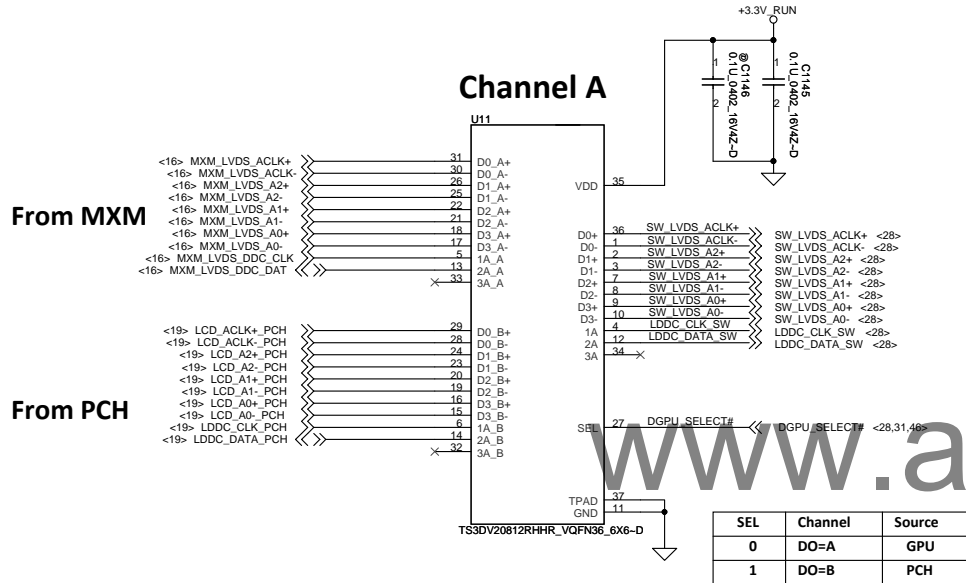
Compal Electronics, Inc.

Current Sensor

LA-7933

Rev 0.2

Date: Wednesday, November 09, 2011 Sheet 26 of 65



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Compal Electronics, Inc.

LVDS SW

LA-7933

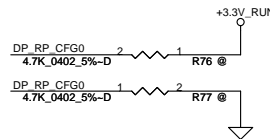
Rev 0.2

Date: Monday, November 07, 2011

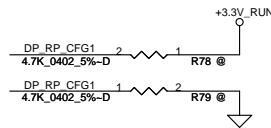
Sheet 27 of 65

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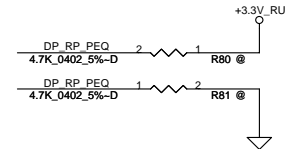




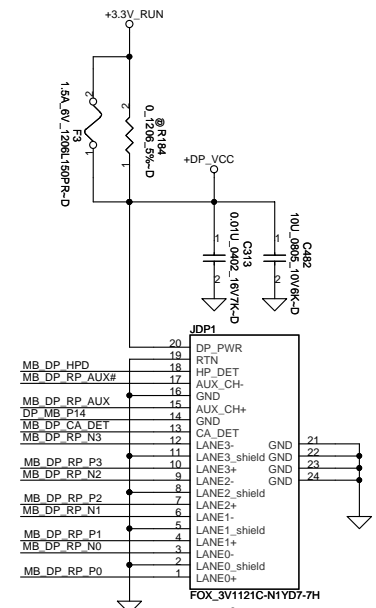
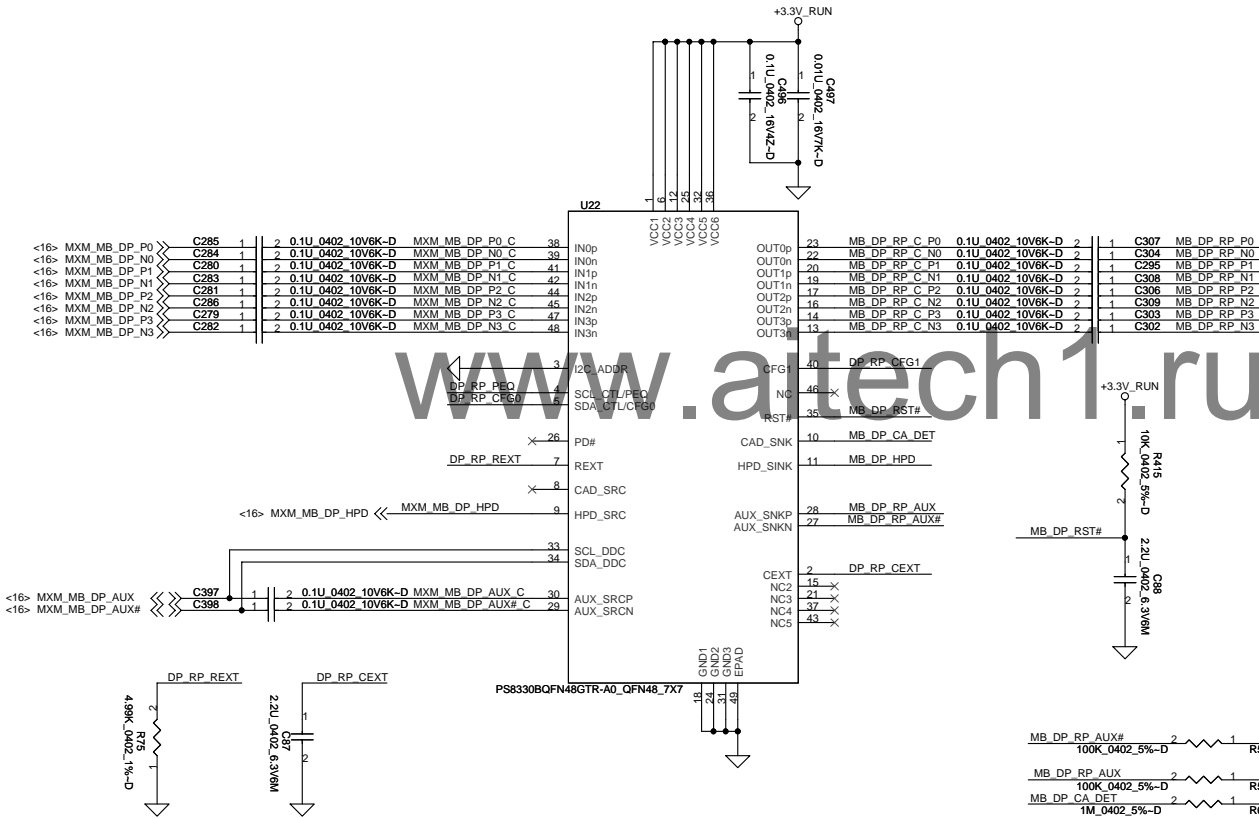
Configuration pin for automatic EQ and AUX interception; Internal pull down at ~150kΩ, 3.3V I/O.  
 L: default, automatic EQ enable & AUX interception enable  
 H: automatic EQ disable & AUX interception enable  
 M: automatic EQ disable & AUX interception disable, no pre-emphasis, 600mVpp swing



Configuration pin for auto test and input offset cancellation, 3.3V IO, internal pull up at ~150K  
 H: default, auto test disable & input offset cancellation enable  
 L: auto test enable & input offset cancellation enable  
 M: auto test disable & input offset cancellation disable



Programmable input equalization levels; Internal pull down at ~150kΩ, 3.3V I/O.  
 L: default, LEQ, compensate channel loss up to 12dB @ HBR2  
 H: HEQ, compensate channel loss up to 15dB @ HBR2  
 M: LLEQ, compensate channel loss up to 5dB @ HBR2

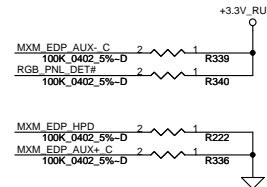
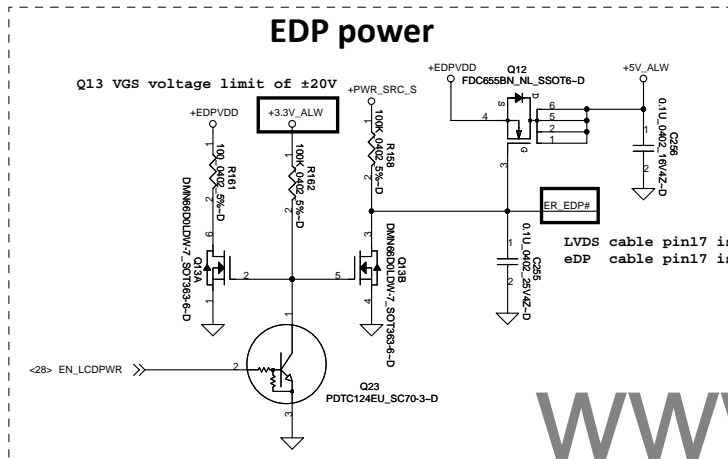


Link CIS  
 Vendor change MPN to 3V11211-NBYD7-7H  
 but no modif PCB footprint

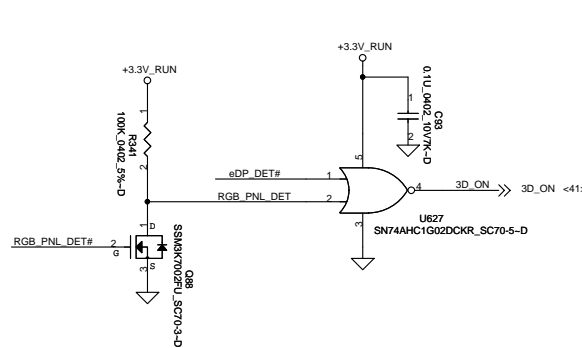
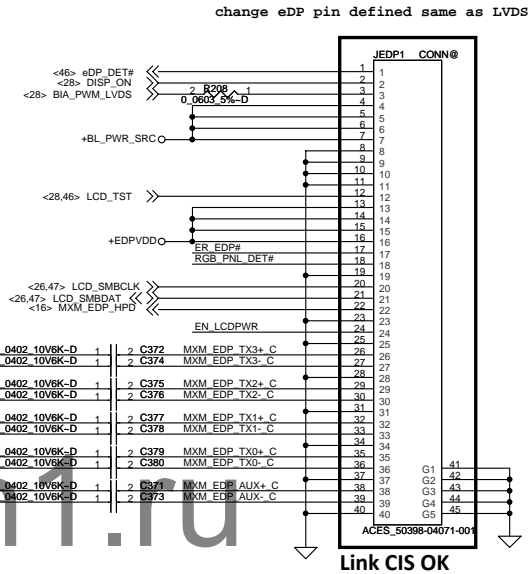
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Title DP CONN			
Size	Document Number LA-7933	Rev 0.2	
Date	Monday, November 07, 2011	Sheet	29 of 85

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LVDS cable pin17 is GND and  
edp cable pin17 is floating(ER\_EDP#)



	EDP_DET#	RGB_DET#	3D_ON
RGB panel	0	1	0
3D panel	0	0	1
LVDS panel	1	0	0

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**Compal Electronics, Inc.**

**EDP CONN**

File: **LA-7933**

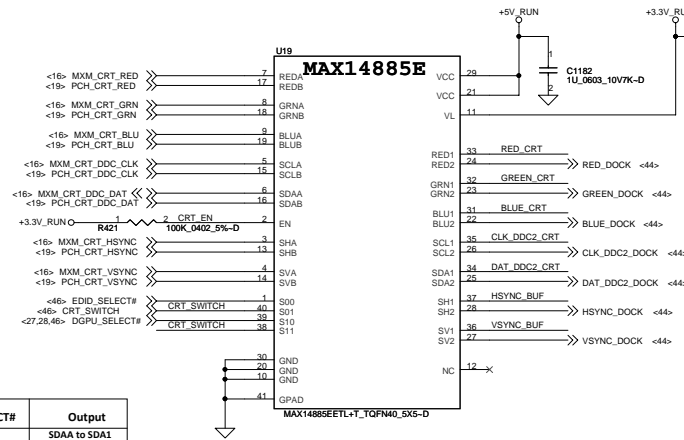
Size: **Monday, November 07, 2011**

Sheet: **30** of **65**

Rev: **0.2**

Channel A --> GPU

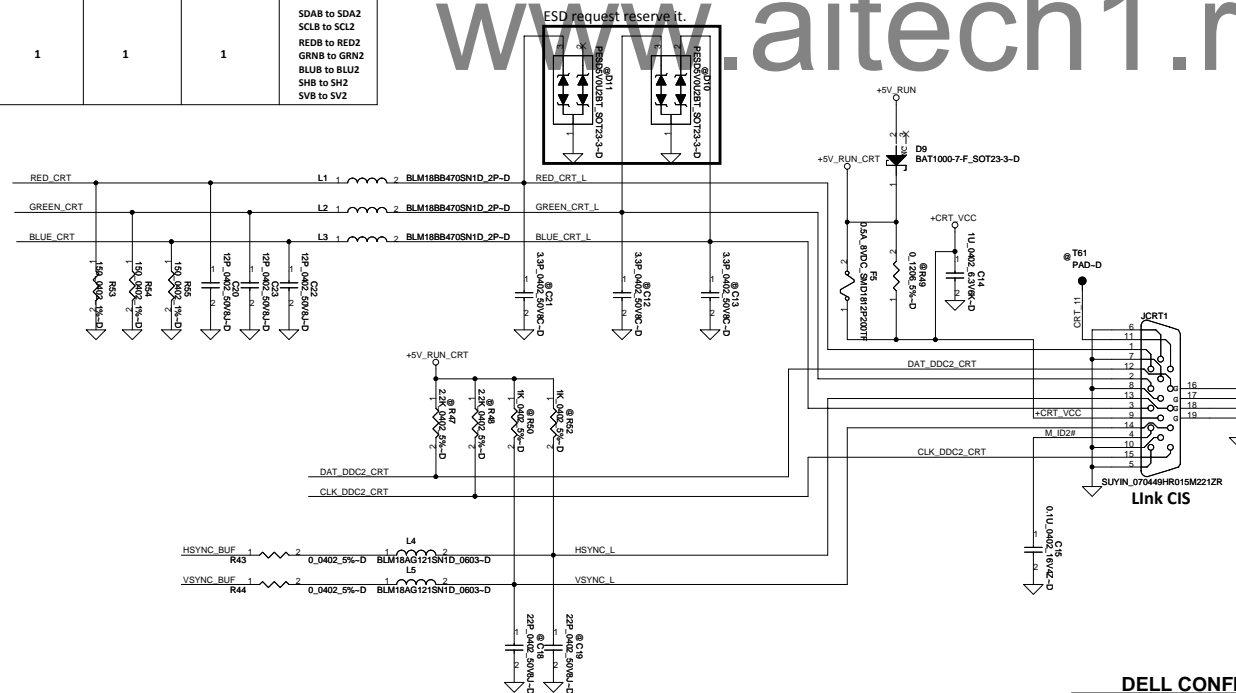
Channel B --> PCH



Port 1 --> MB board CRT

Port 2 --> Docking Port RGB

	CRT_SWITCH	DGPU_SELECT#	EDID_SELECT#	Output
DSC mode output to MB VGA	0	0	0	SDAA to SDA1 SCLA to SCL1 REDA to RED1 GRNA to GRN1 BLUA to BLU1 SHA to SH1 SVA to SV1
DSC mode output to docking VGA	1	0	0	SDAA to SDA2 SCLA to SCL2 REDA to RED2 GRNA to GRN2 BLUA to BLU2 SHA to SH2 SVA to SV2
UMA mode output to MB VGA	0	1	1	SDAB to SDA1 SCLB to SCL1 REDB to RED1 GRNB to GRN1 BLUB to BLU1 SHB to SH1 SVB to SV1
UMA mode output to docking VGA	1	1	1	SDAB to SDA2 SCLB to SCL2 REDB to RED2 GRNB to GRN2 BLUB to BLU2 SHB to SH2 SVB to SV2



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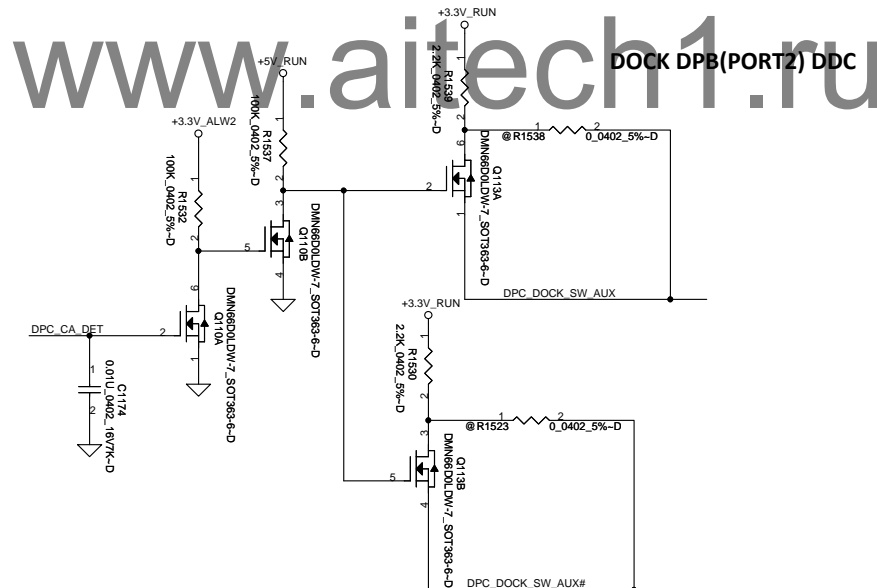
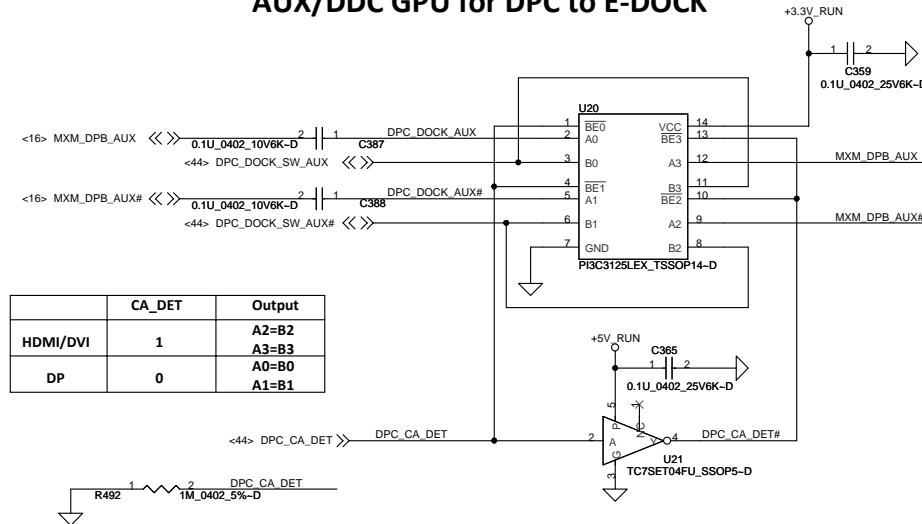


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File	VGA_CONN
Doc Number	LA-7933
Date	Tuesday, November 08, 2011
Sheet	31 of 65

## AUX/DDC GPU for DPC to E-DOCK



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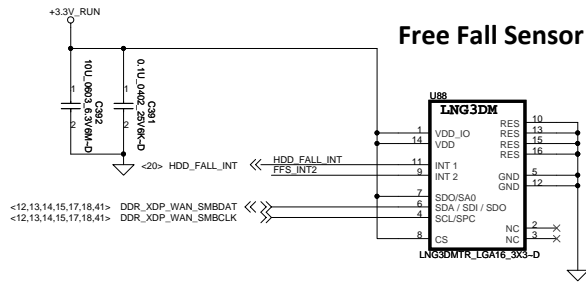
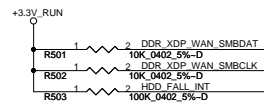
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Title			
DP DDC SW			
Size	Document Number		Rev
	LA-7933		0.2
Date:	Monday, November 07, 2011		Sheet 32 of 65

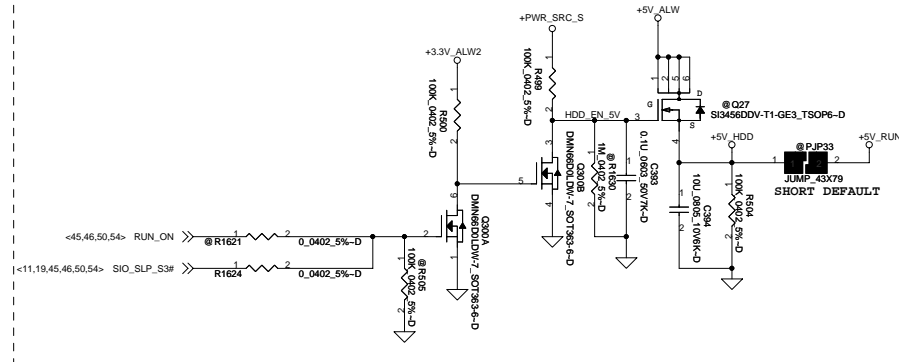
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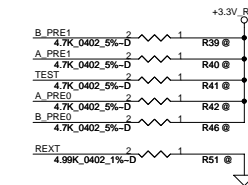
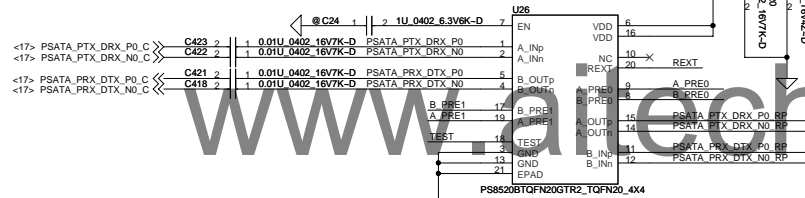




## HDD PWR



## HDD Repeater

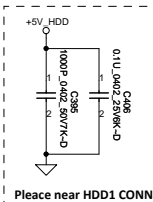
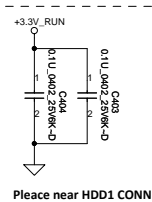
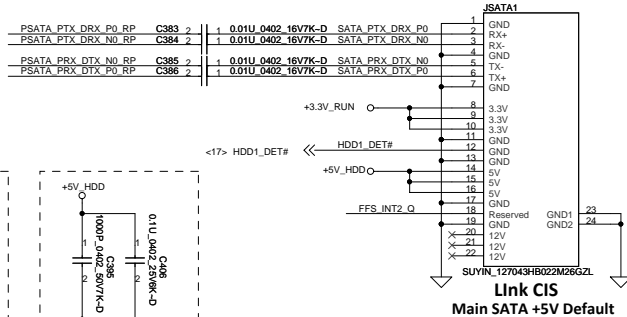


Pre-emphasis level setting for Channel A,  
3.3V tolerant. Internally pulled down at ~150KΩ  
[A\_PRE1, A\_PRE0] ==  
00: 0dB, no pre-emphasis  
01: 1.5dB pre-emphasis is selected  
10: 2.5dB pre-emphasis is selected  
11: 3.5dB pre-emphasis is selected

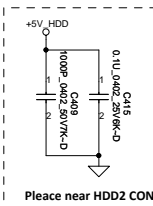
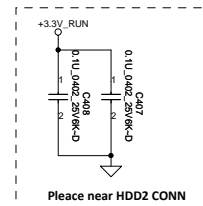
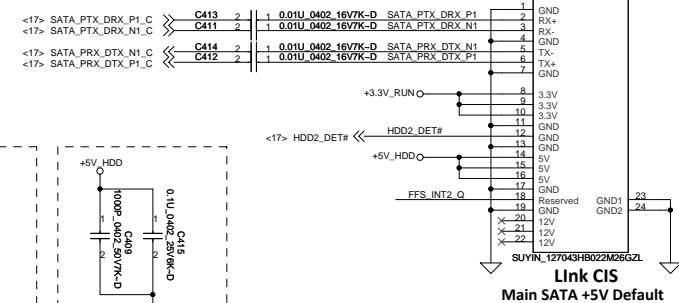
Pre-emphasis level setting for Channel B,  
3.3V tolerant. Internally pulled down at ~150KΩ  
[B\_PRE1, B\_PRE0] ==  
00: 0dB, no pre-emphasis  
01: 1.5dB pre-emphasis is selected  
10: 2.5dB pre-emphasis is selected  
11: 3.5dB pre-emphasis is selected

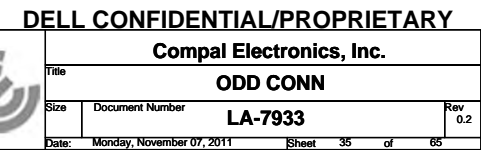
Chip test mode enable, internally pulled down at ~150KΩ  
L: Normal operation  
H: Test mode enable  
For SATA/SAS PHY test, this pin should be pulled to High

## HDD1 CONN

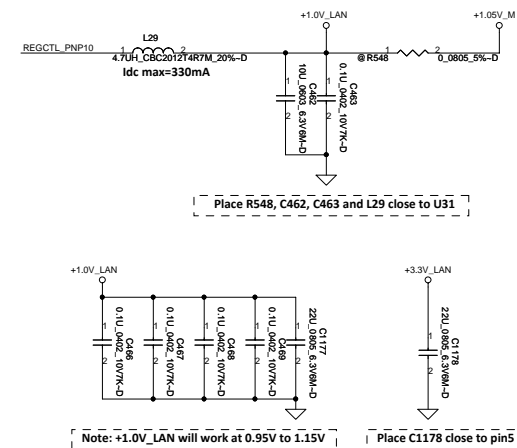


## HDD2 CONN



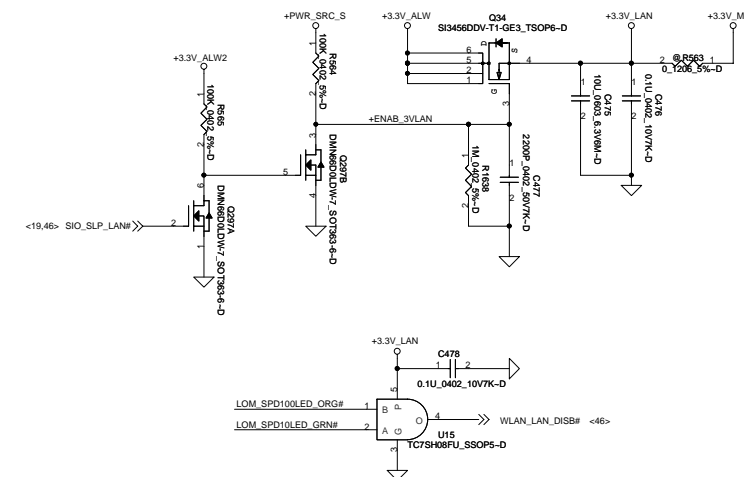
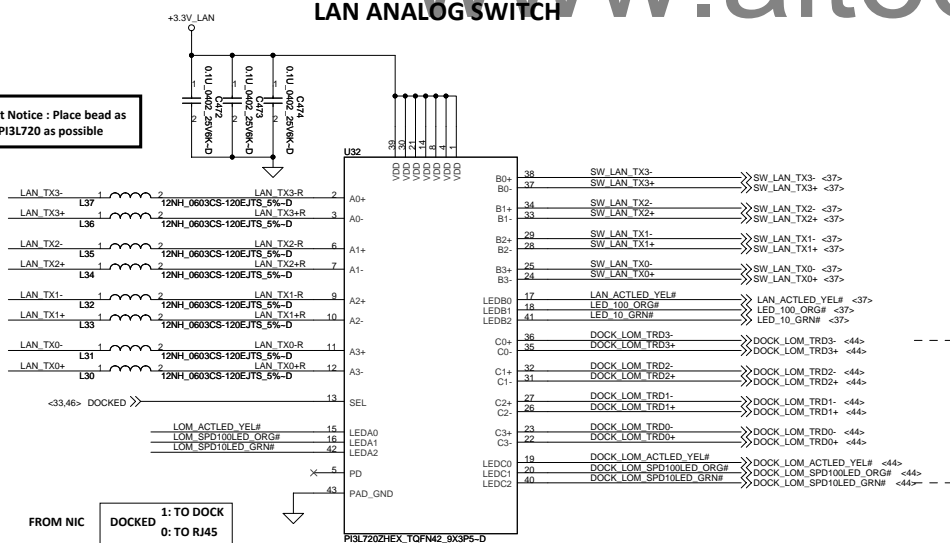


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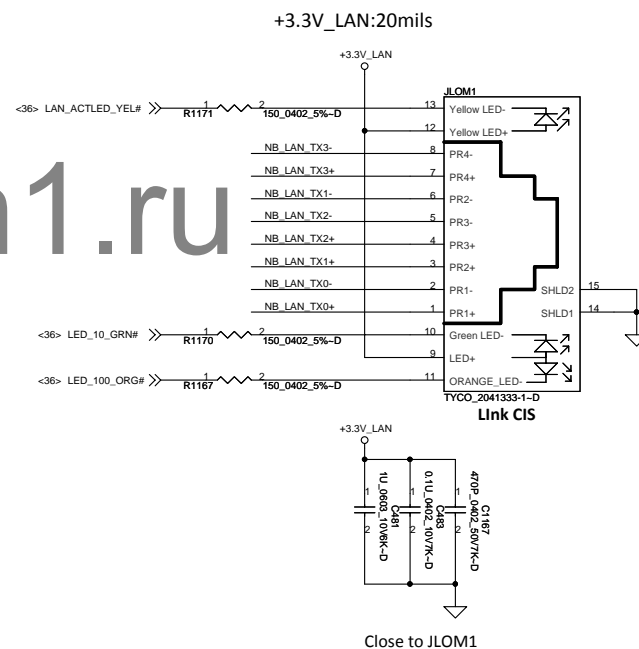
+1.0V_LAN POWER OPTIONS	
Shared with PCH 1.05V SVR	* Internal SRV
STUFF: R548 NO STUFF: L29	STUFF: L29 NO STUFF: R548

**Layout Notice : Place bead as close PI3L720 as possible**



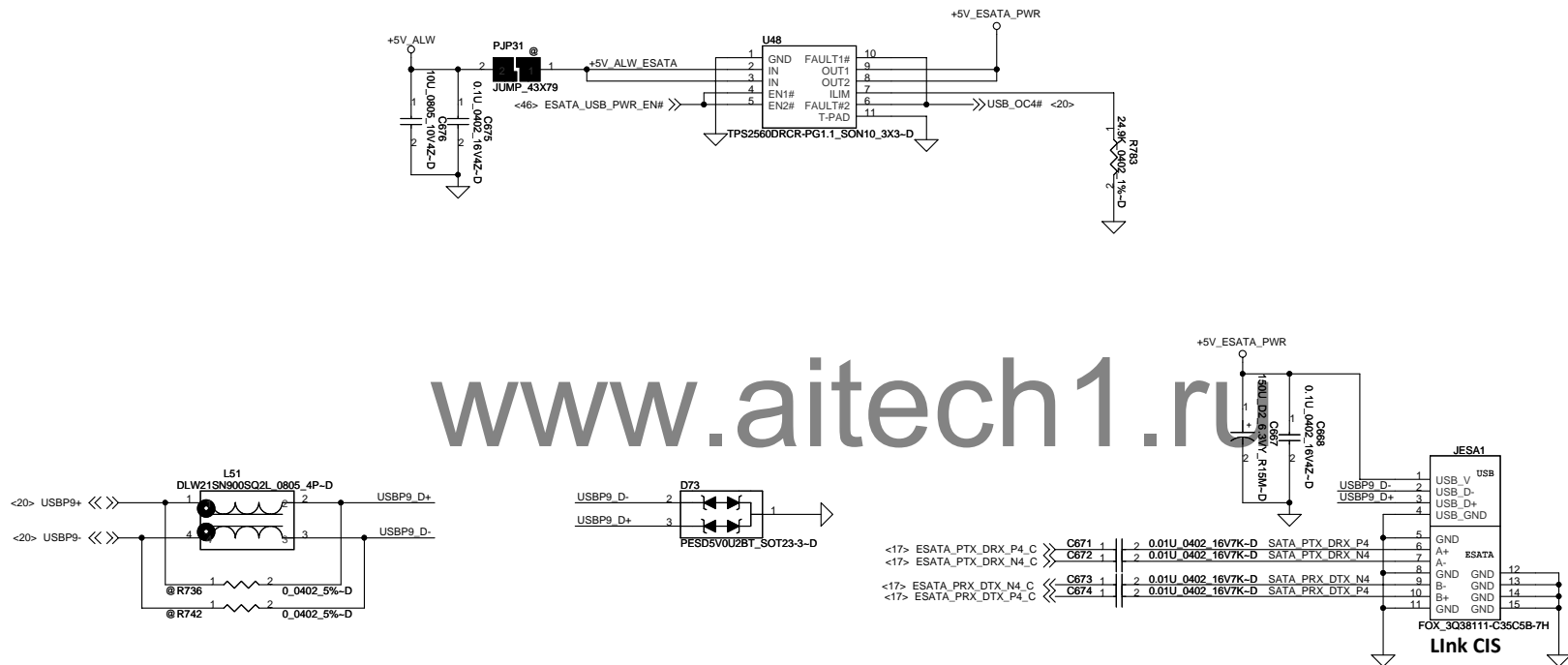
Date: Monday, November 07, 2011 Sheet 36 of 65

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Title			
RJ45			
Size	Document Number		Rev
	LA-7933		0.2
Date:	Monday, November 07, 2011	Sheet 37 of 65	

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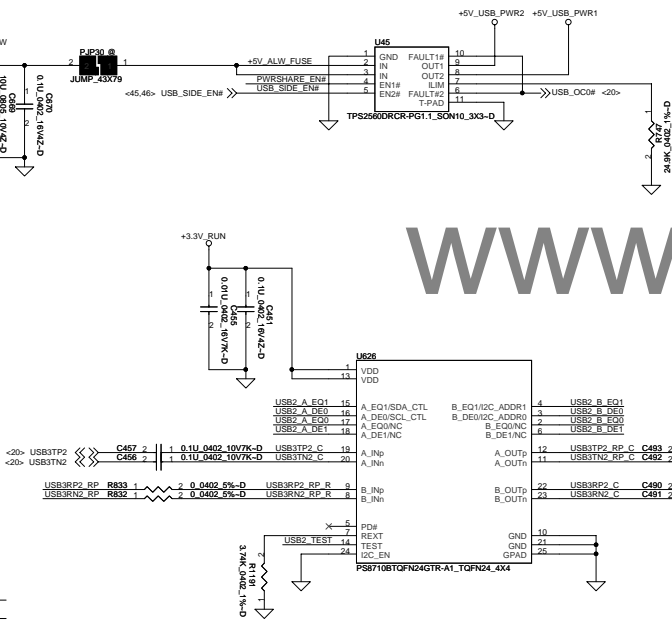
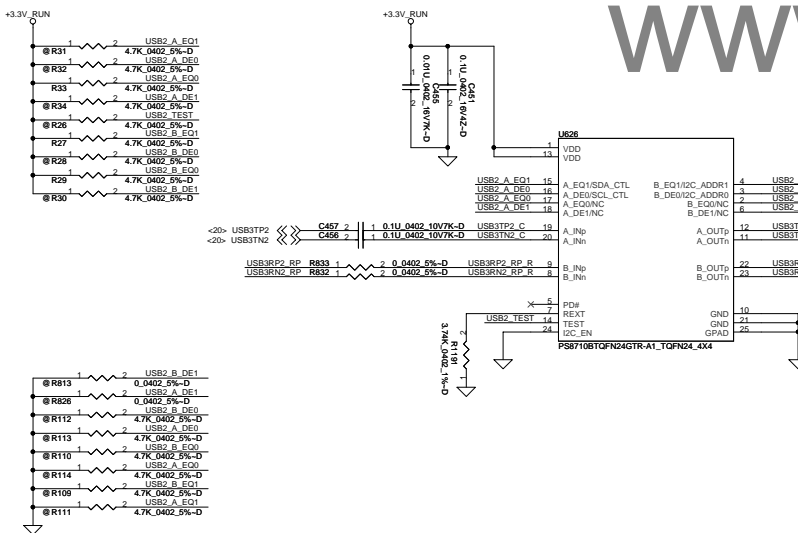
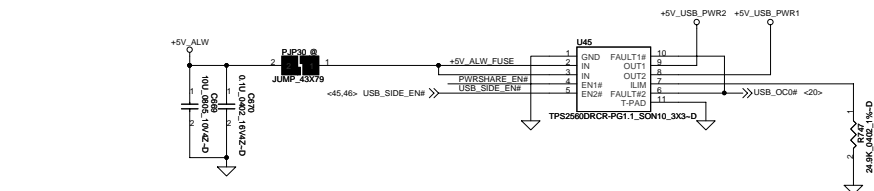
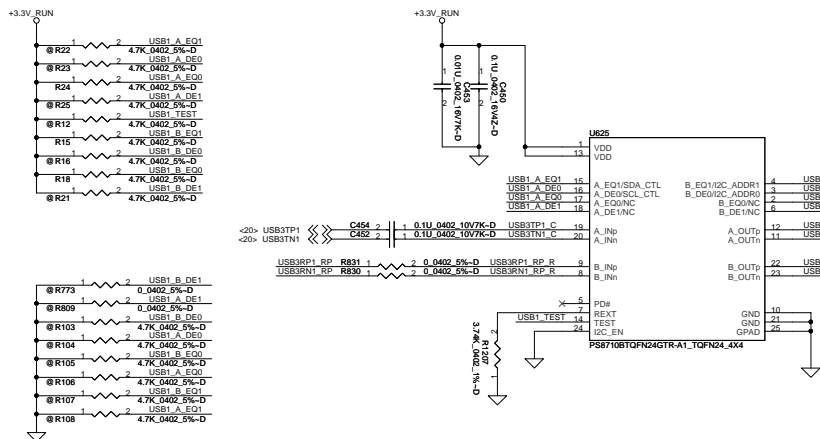
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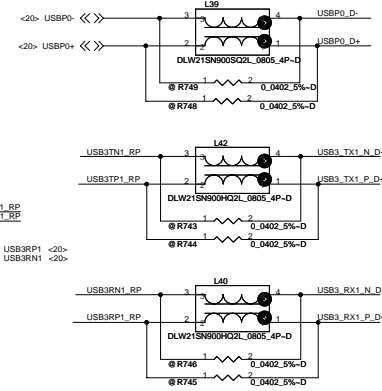


Title			ESATA
Size	Document Number	LA-7933	
Date	Monday, November 07, 2011	Sheet	38 of 65
Rev	0.2		

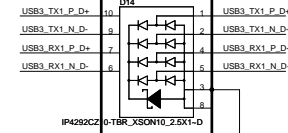
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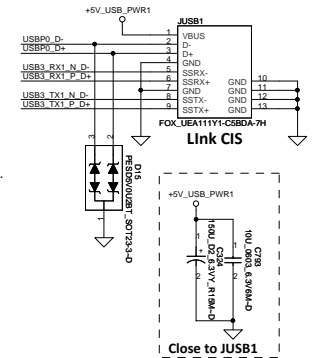
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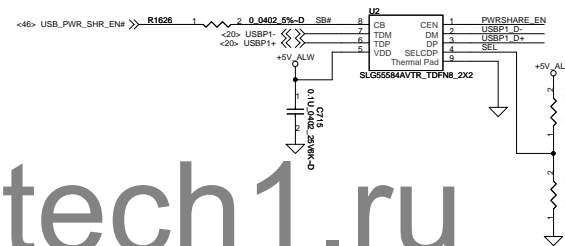
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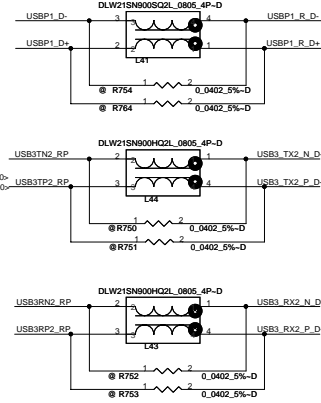
ESD request change main source to SC300002FOL.



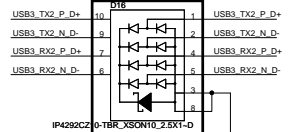
#### Power share SW



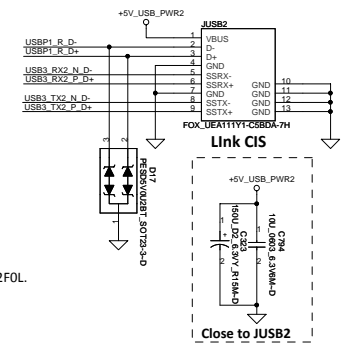
#### For EMI request



#### For ESD request



ESD request change main source to SC300002FOL.



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USB3.0

File	Document Number	Rev
LA-7933	LA-7933	0.2
Date	Friday, November 11, 2011	Sheet 39 of 85

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**Mini WWAN/GPS/LTE H= 4 mm**

The figure illustrates the electrical interface for the Mini WWAN/GPS/LTE H= 4 mm module. It includes a detailed pinout and connection diagram, a simplified connection diagram to a Link CIS, and a power specification table.

**Power Specifications Table:**

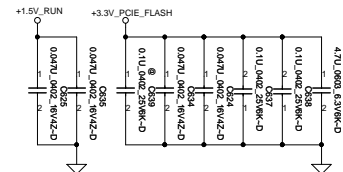
PWR Rail	Voltage Tolerance	Primary Power		Aux Power
		Peak	Normal	Normal
+3.3V	+9%	1000	750	
+3.3Vaux	+9%	330	250	250 (Wake enable) 150 (Not wake enable)
+1.5V	+5%	500	375	NA

FWR Rail	Voltage Tolerance	Primary Power		Aux Power
		Peak	Normal	Normal
+3.3V	+ -9%	1000	750	
+3.3Vaux	+ -9%	330	250	250 (Wake enable) 5 (Not wake enable)
+1.5V	+ -5%	500	375	NA

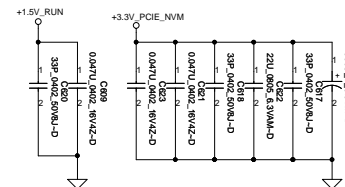
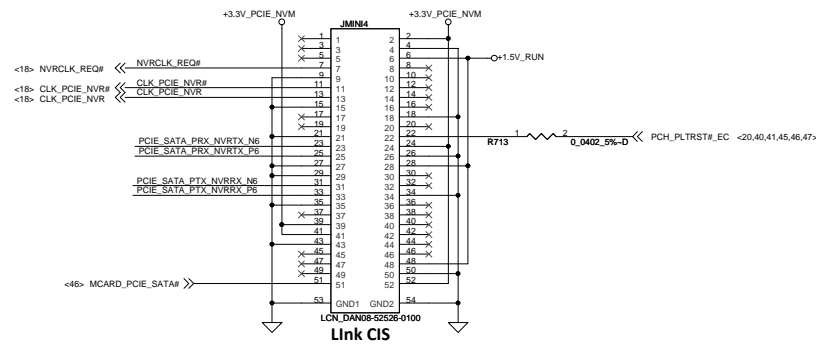
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[illegible]

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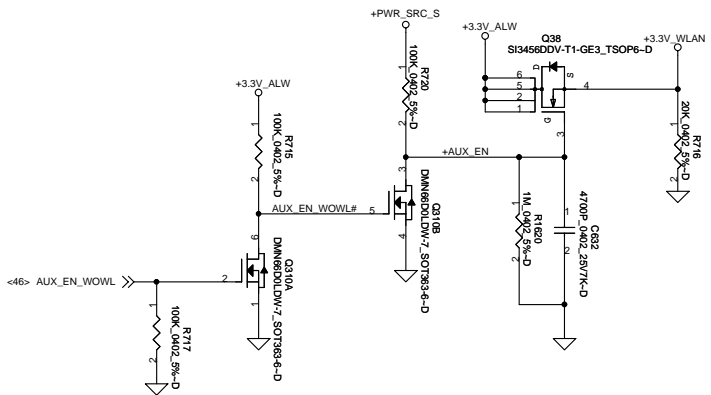
**Compal Electronics, Inc.**

**LA-7933**

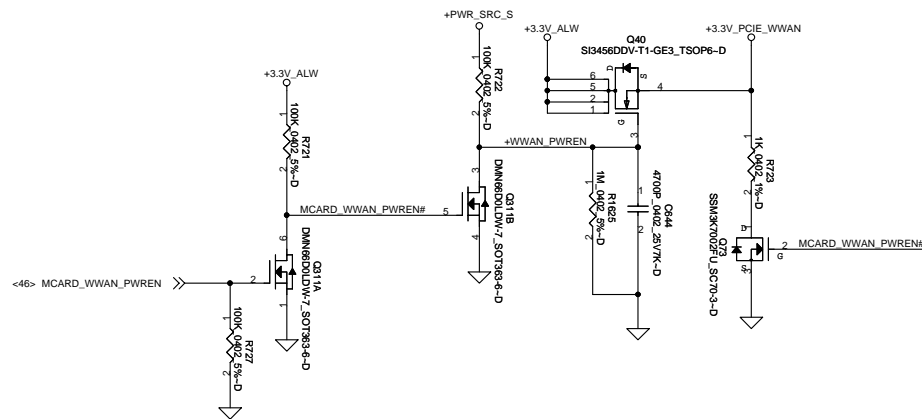
Date: Monday, November 07, 2011 Sheet 42 of 65

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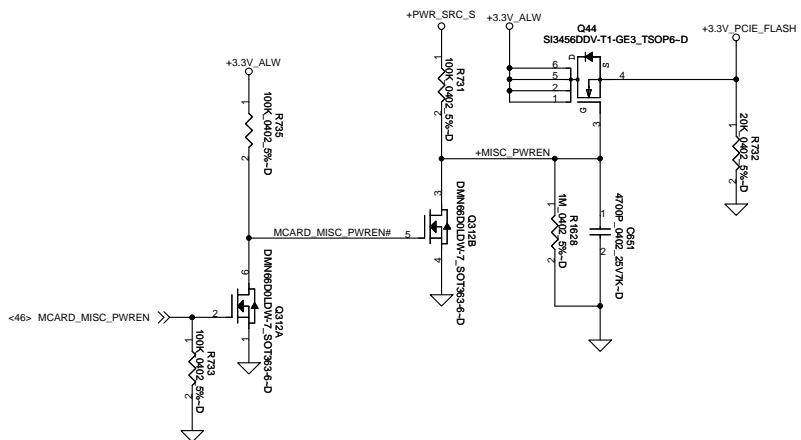
## Power Control for Mini card1



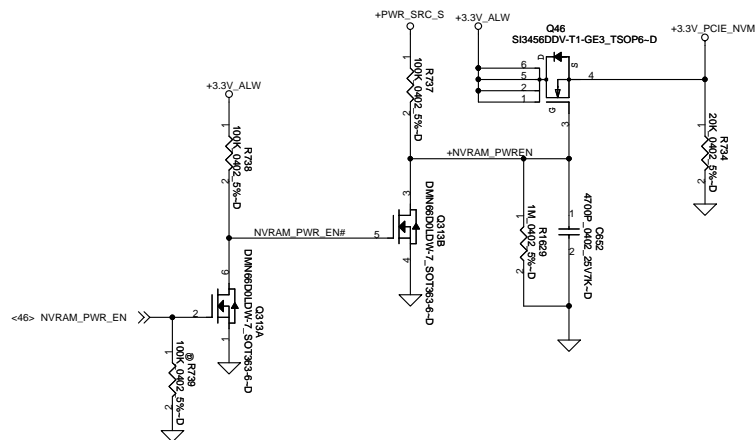
## Power Control for Mini card2



## Power Control for Mini card3



## Power Control for Mini card4



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### Mini Card PWR

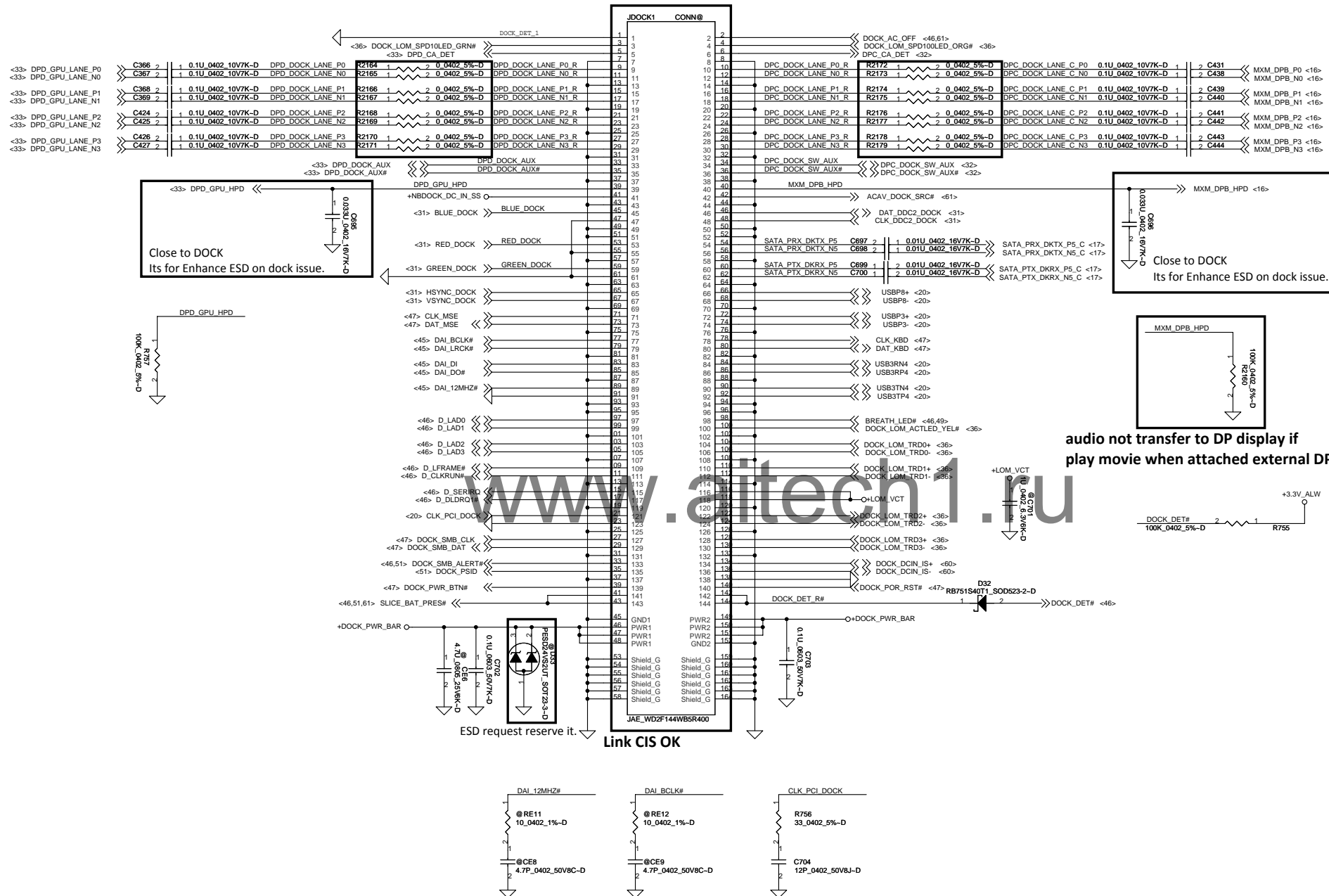
Size	Document Number
Date:	Monday, November 07, 2011

7933

Sheet 43 of

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EMI request add 33ohm for DOCK DVI signals.



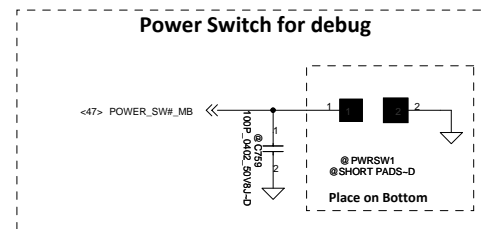
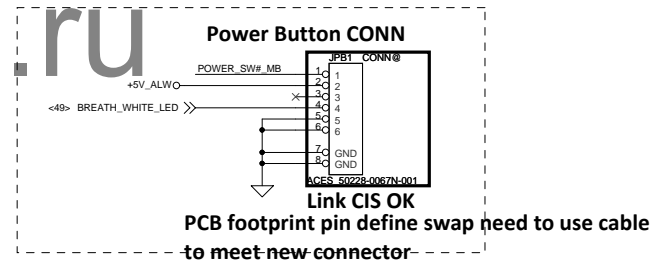
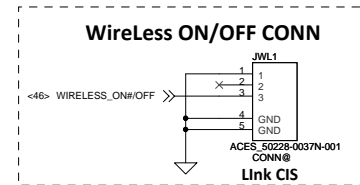
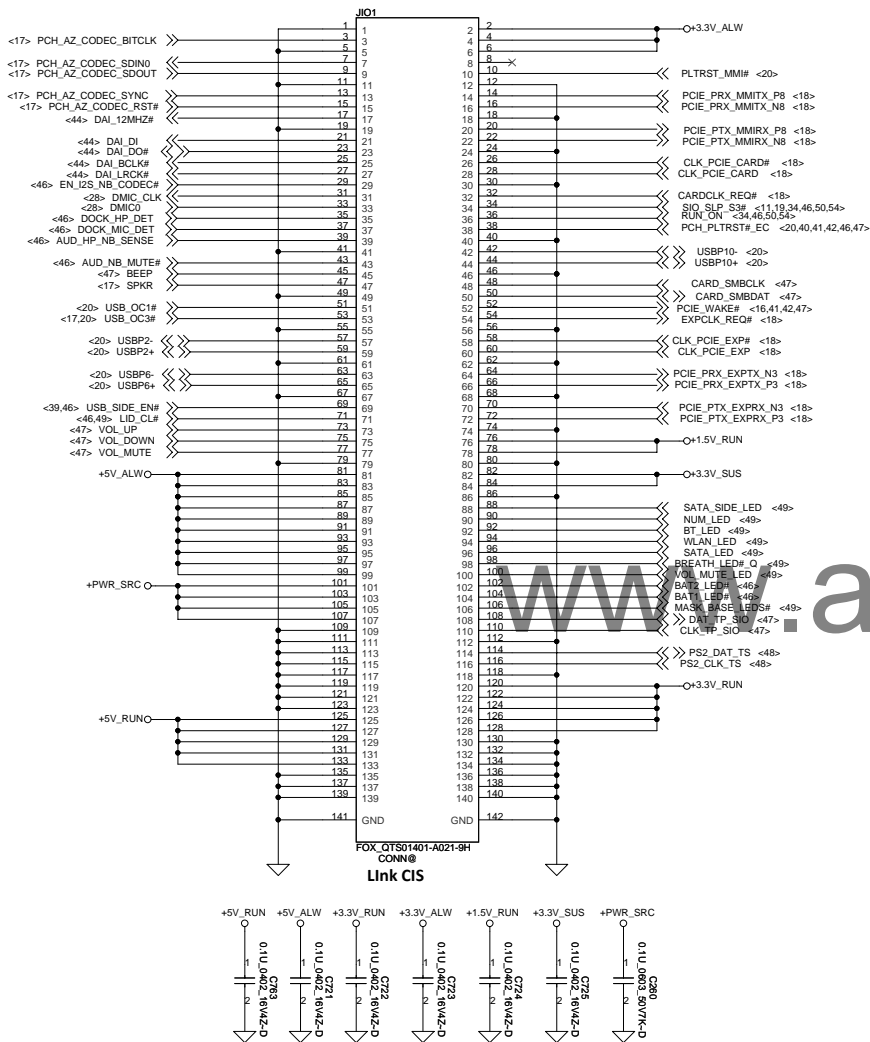
**audio not transfer to DP display if  
play movie when attached external DP display**

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Title			
<b>Docking</b>			
Size	Document Number		Rev
	<b>LA-7933</b>		<b>0.2</b>
Date:	Friday, November 11, 2011		Sheet 44 of 85

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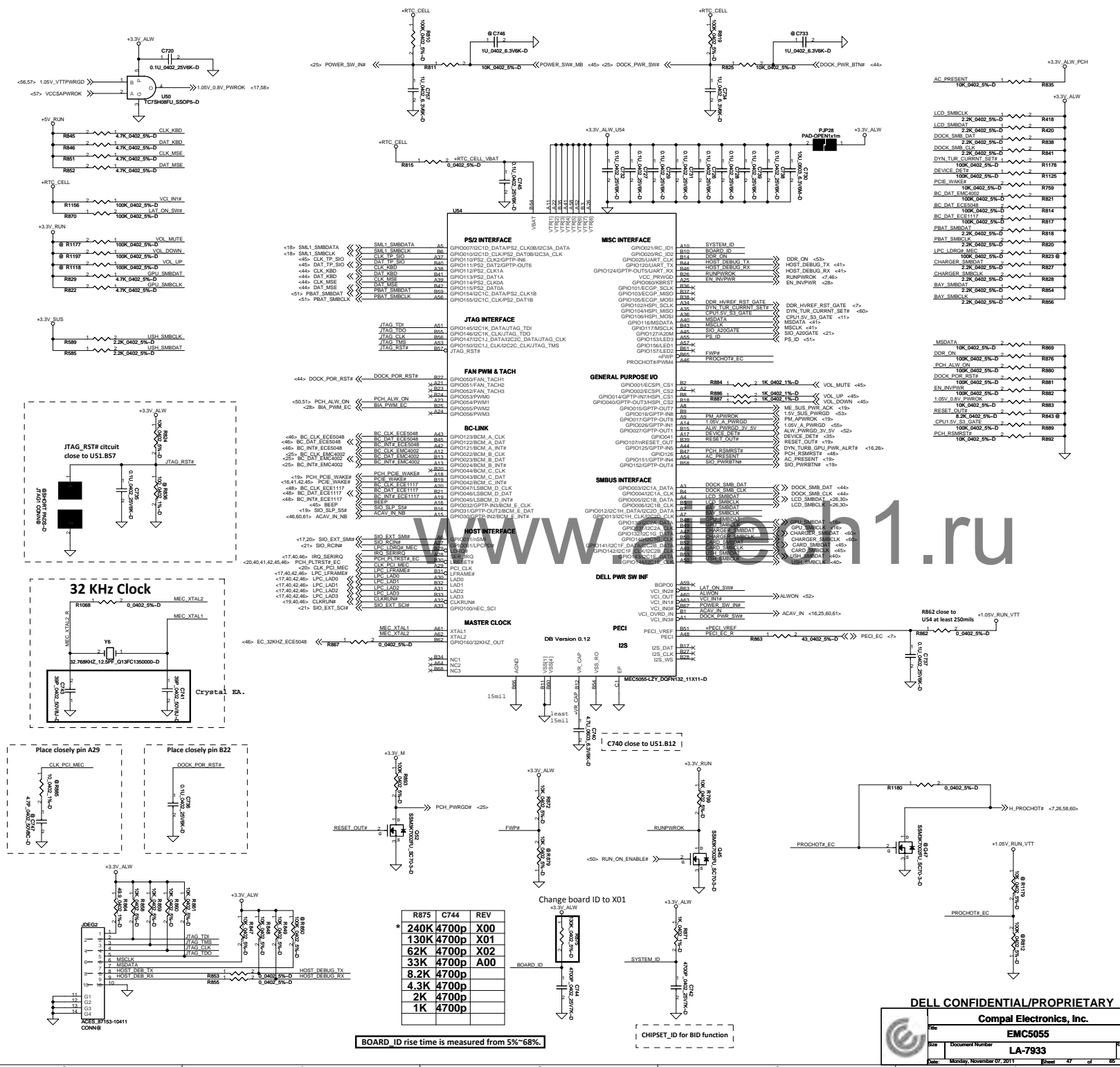
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File		I/O board	
Size		Document Number	
		LA-7933	
Date:		Monday, November 07, 2011	
		Sheet 45 of 65	

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LA-7933 Date: Wednesday, November 09, 2011 Sheet 46 of 65 0.2



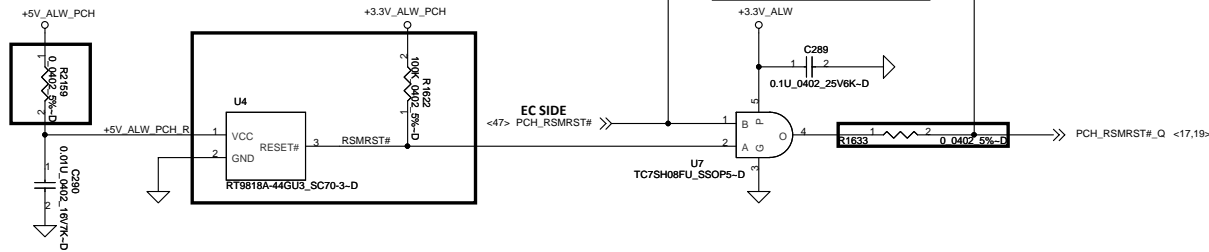
BOARD ID rise time is measured from 5%~68%.

CHIPSET\_ID for BID function

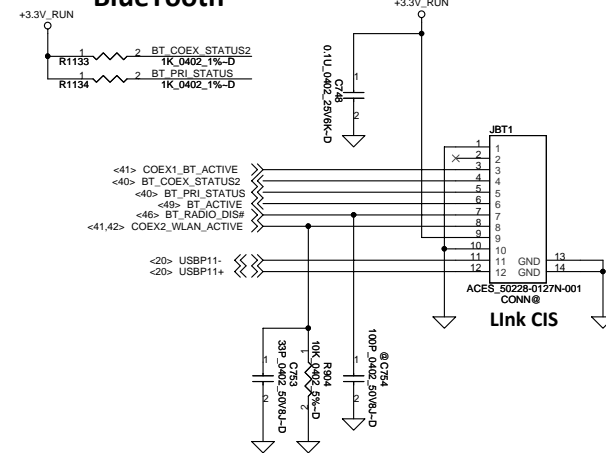
R875	C744	REV
240K	4700p	X00
130K	4700p	X01
62K	4700p	X02
33K	4700p	A00
8.2K	4700p	
4.3K	4700p	
2K	4700p	
1K	4700p	

## RSMRST circuit

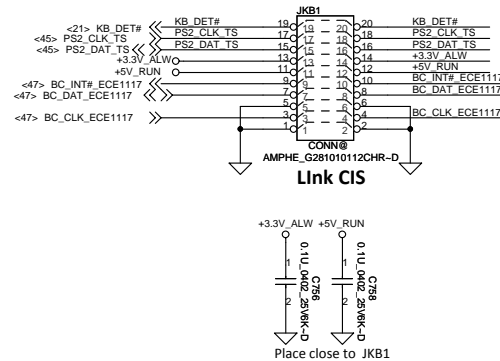
For meet T235(power off)= min 40ns(SPEC).T08a(power on)= max 90ms.



## BlueTooth



## Keyboard



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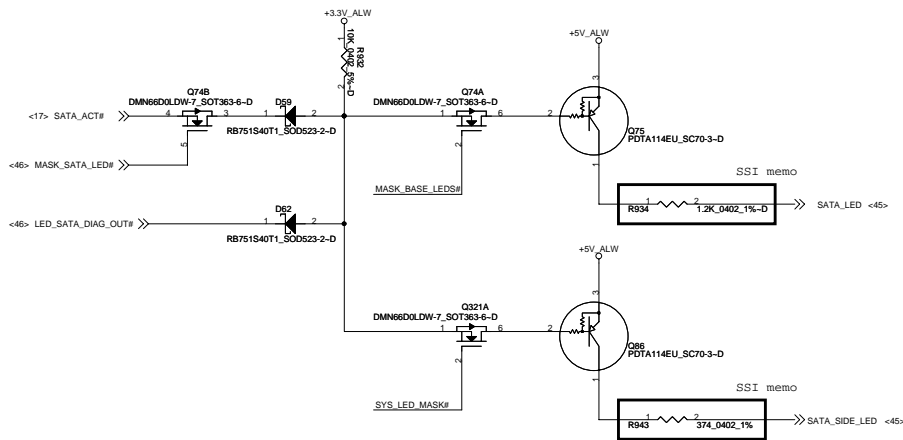
Touch PAD/Int KB

File  
Size  
Date: Monday, November 07, 2011  
Sheet 48 of 85  
Rev 0.2

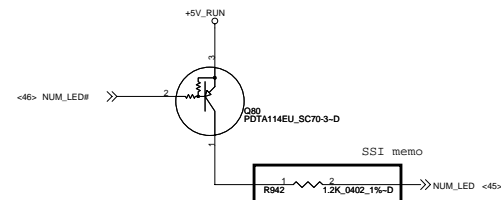
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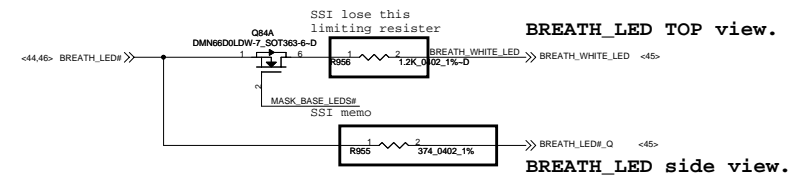
## HDD LED



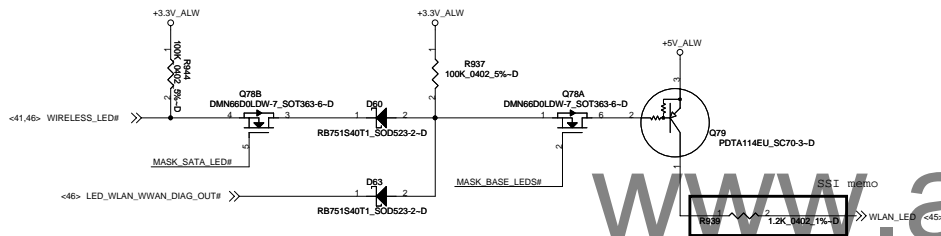
## NUM LED



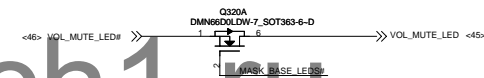
## Breath LED



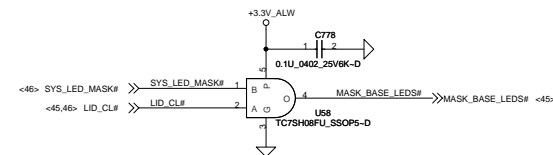
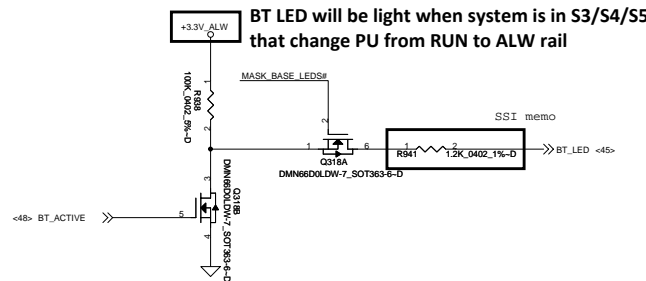
## WWAN/WLAN LED



## Volume mute LED



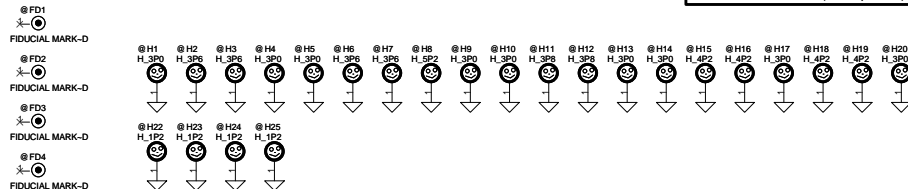
## BT LED



LED Circuit Control Table

	SYS_LED_MASK#	LID_CL#
Mask All LEDs (Sniffer Function)	0	X
Mask Base MB LEDs (Lid Closed)	1	0
Do not Mask LEDs (Lid Opened)	1	1

## Fiducial Mark



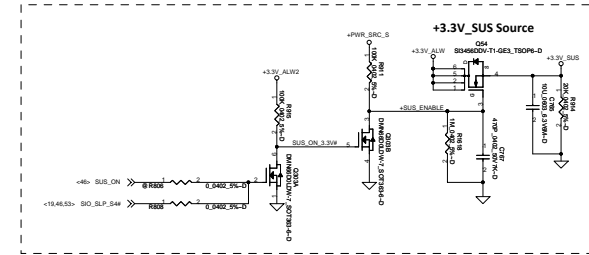
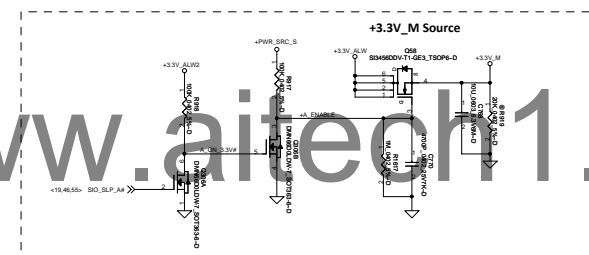
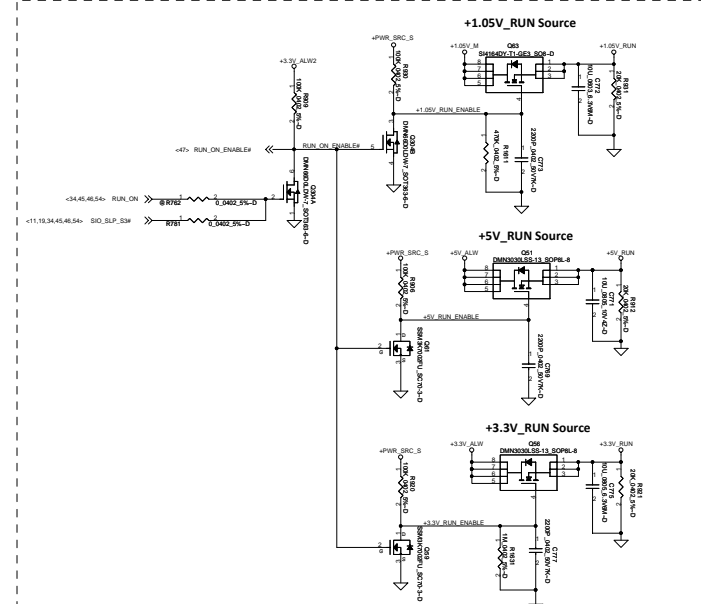
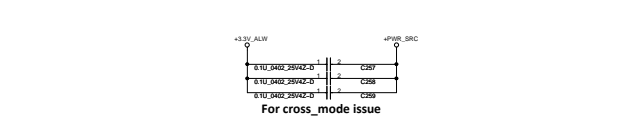
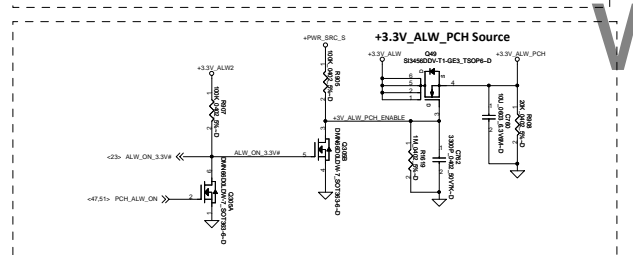
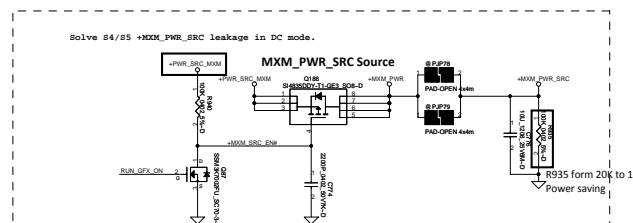
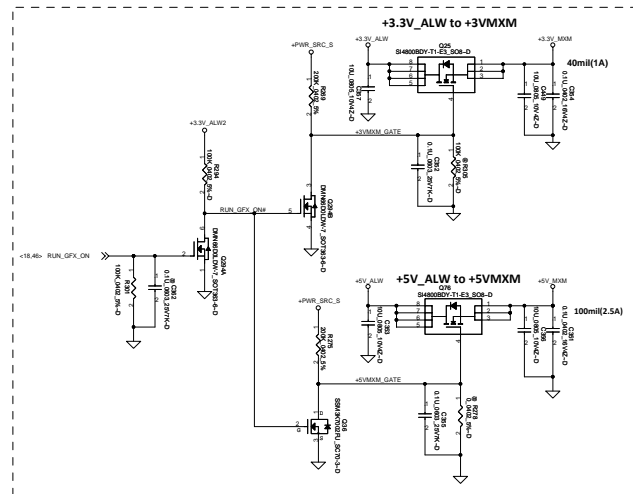
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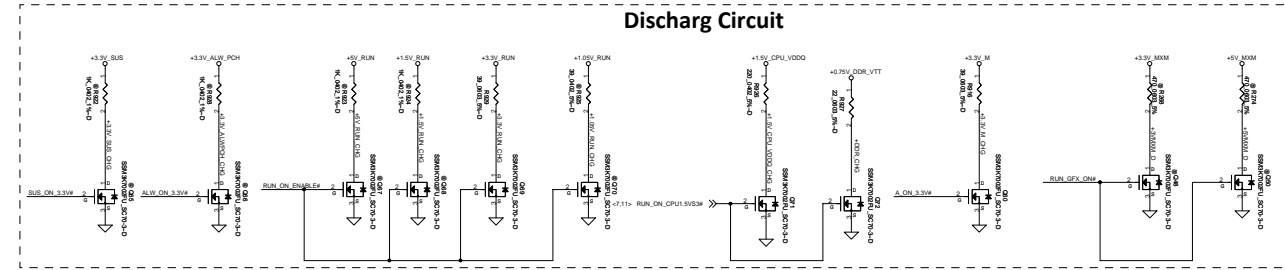
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PAD & Standoff & LED

Size Document Number LA-7933 Rev 02  
Date: Monday, November 07, 2011 Sheet 49 of 65



## Discharge Circuit



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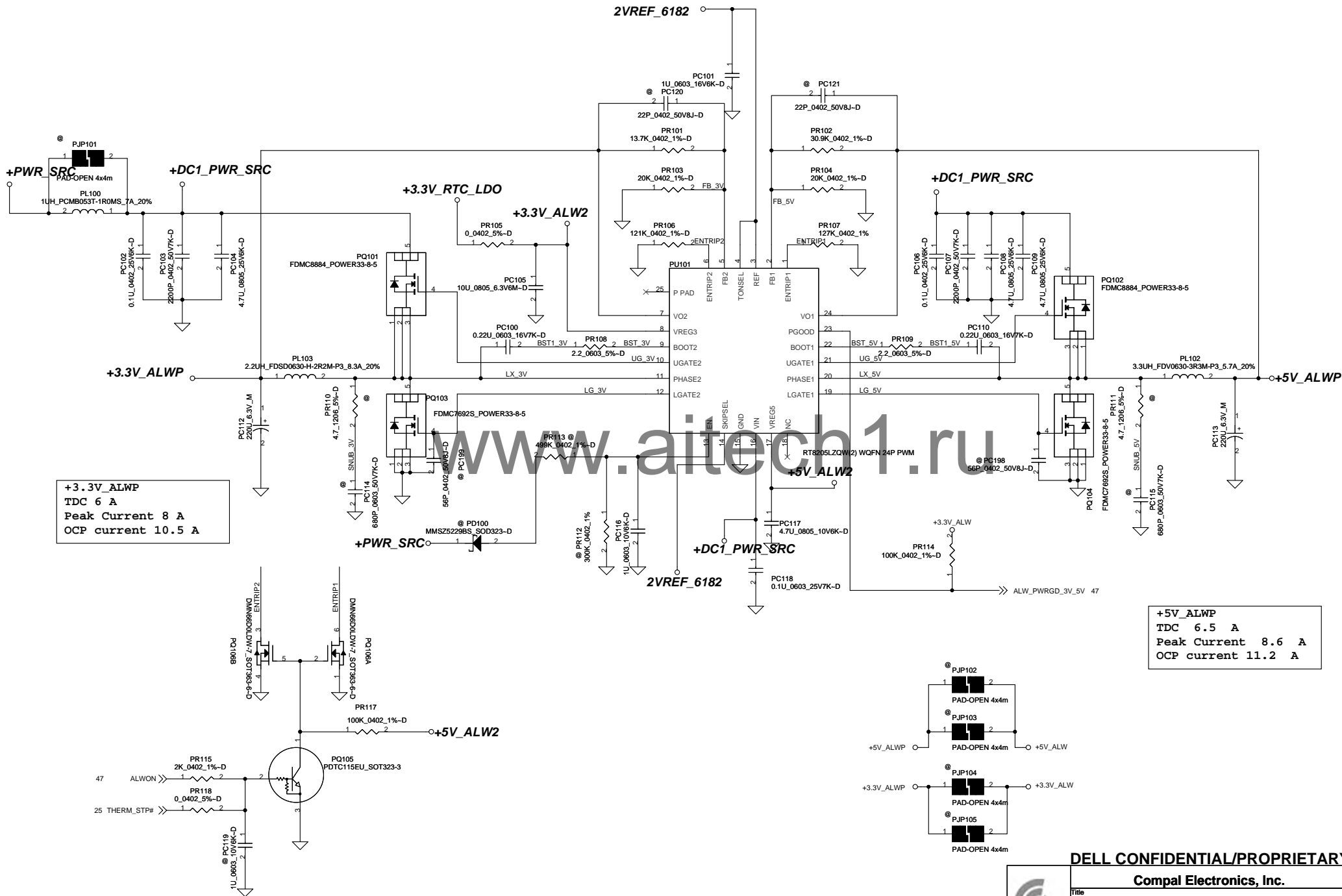
Power Control



LA-7933

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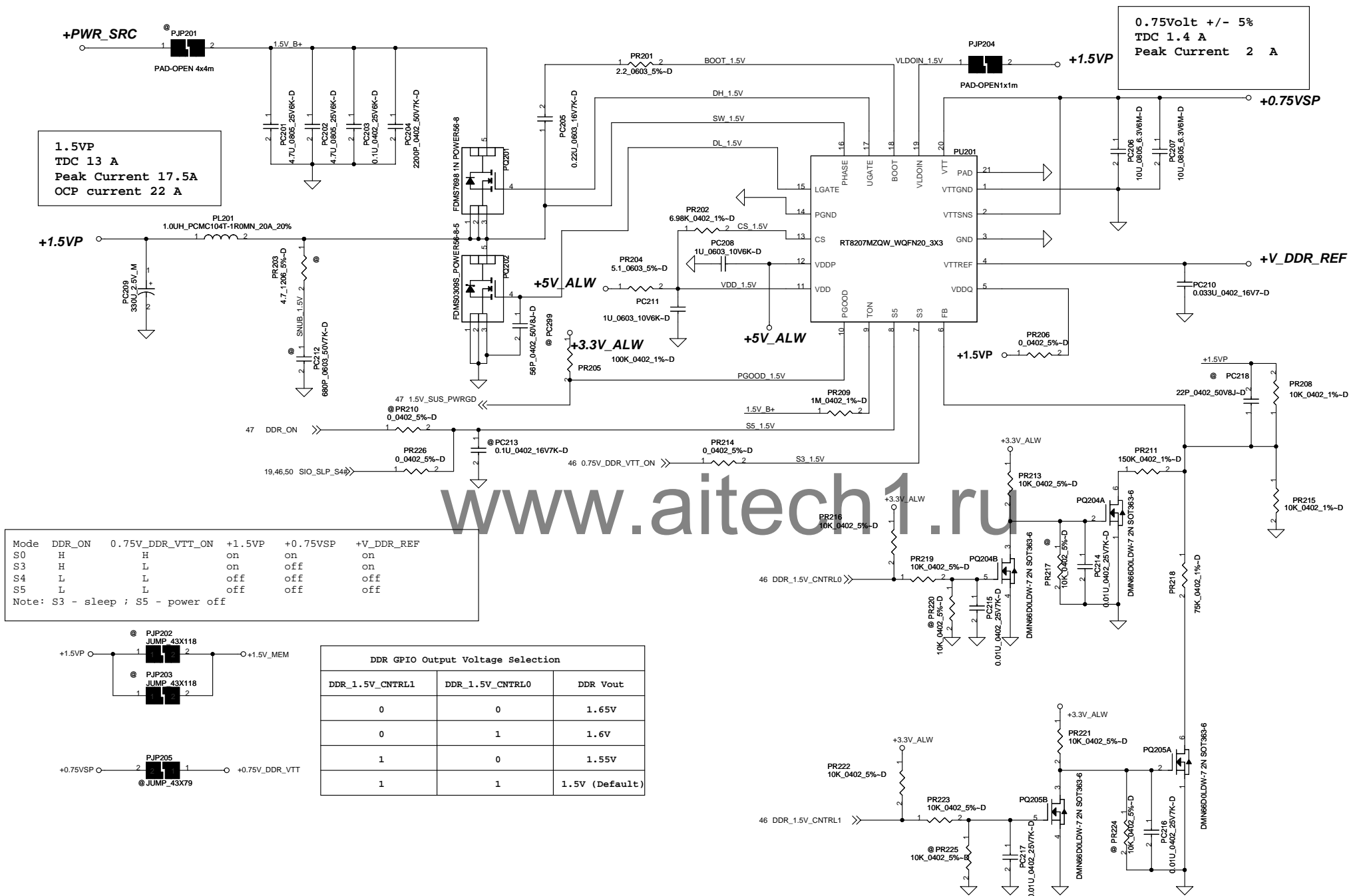


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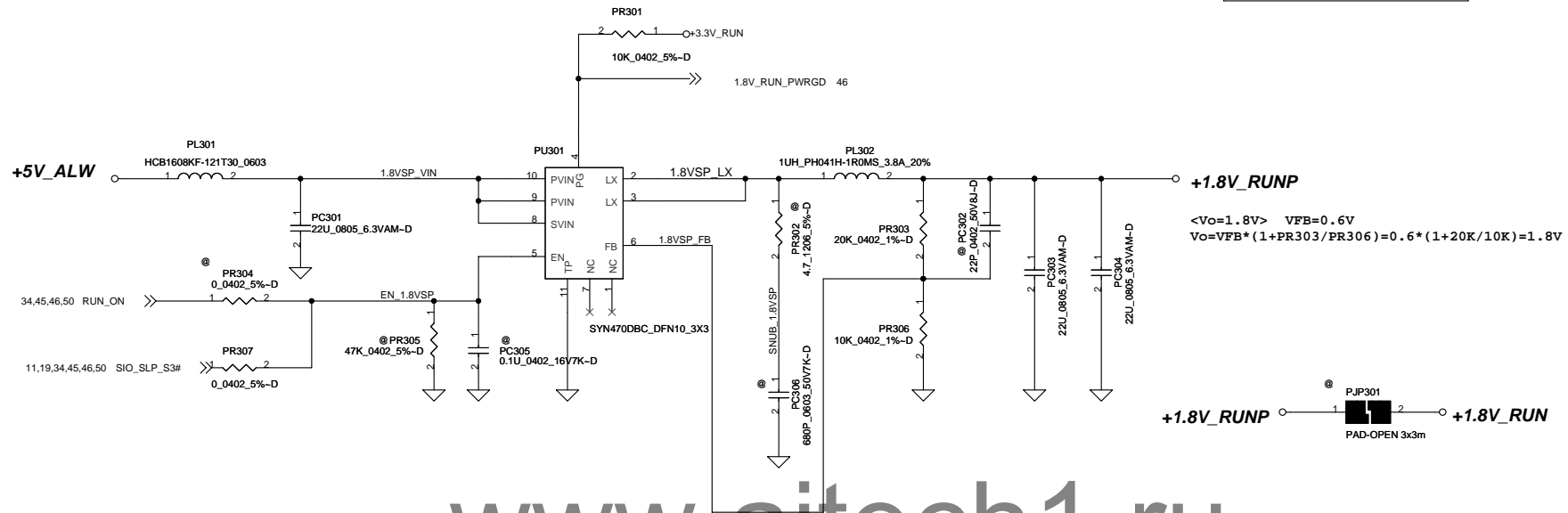
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Size	Document Number	Rev	
LA-7933		0.2	
Date	Monday, November 07, 2011	Sheet	52 of 65

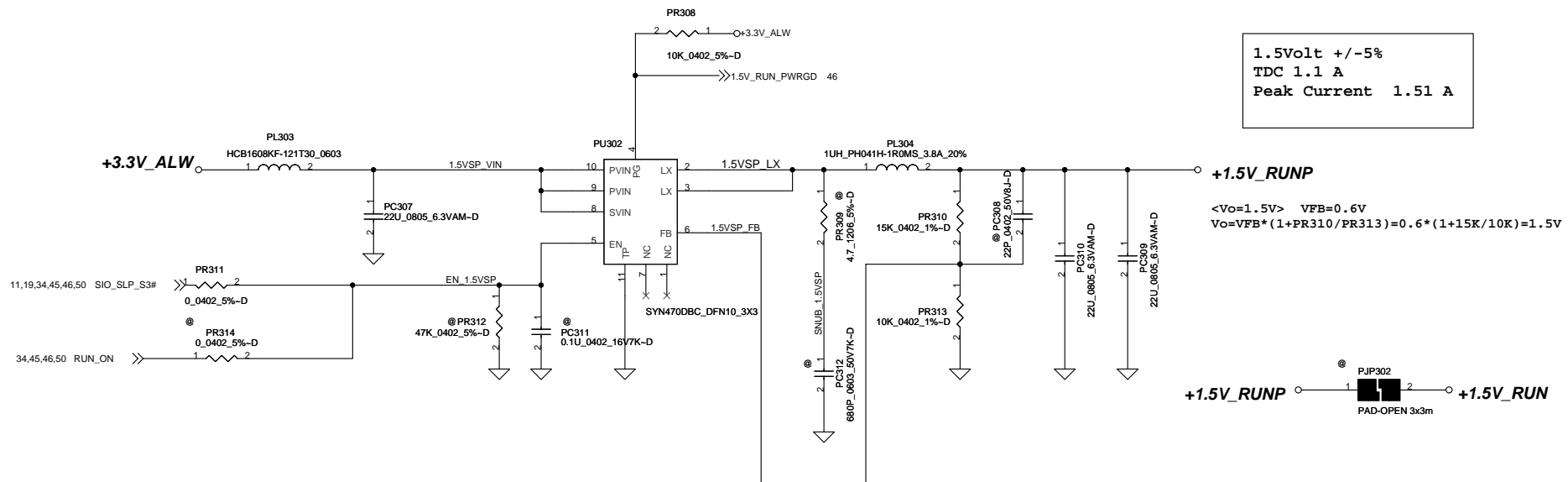


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1.8Volt +/-5%  
TDC 0.65A  
Peak Current 0.93A



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## +1.8V\_RUN

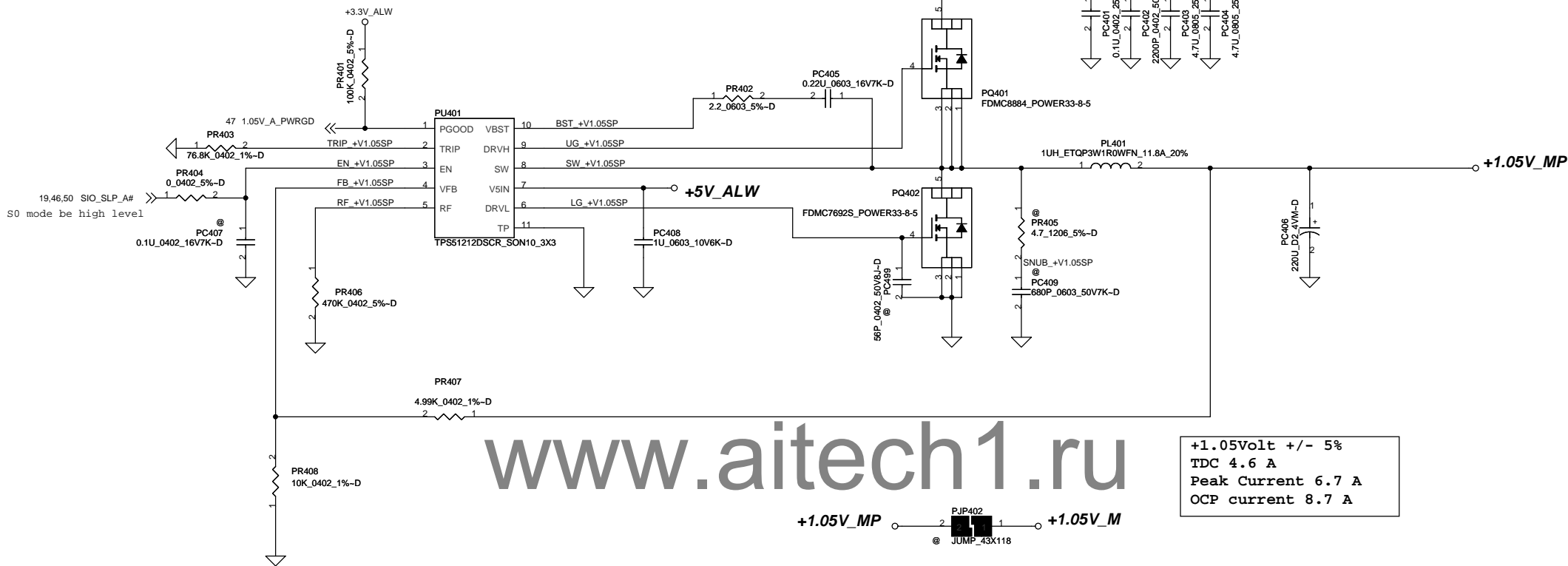
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**LA-7933**

Rev	0.2
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Date: Monday, November 07, 2011 Sheet 54 of 65

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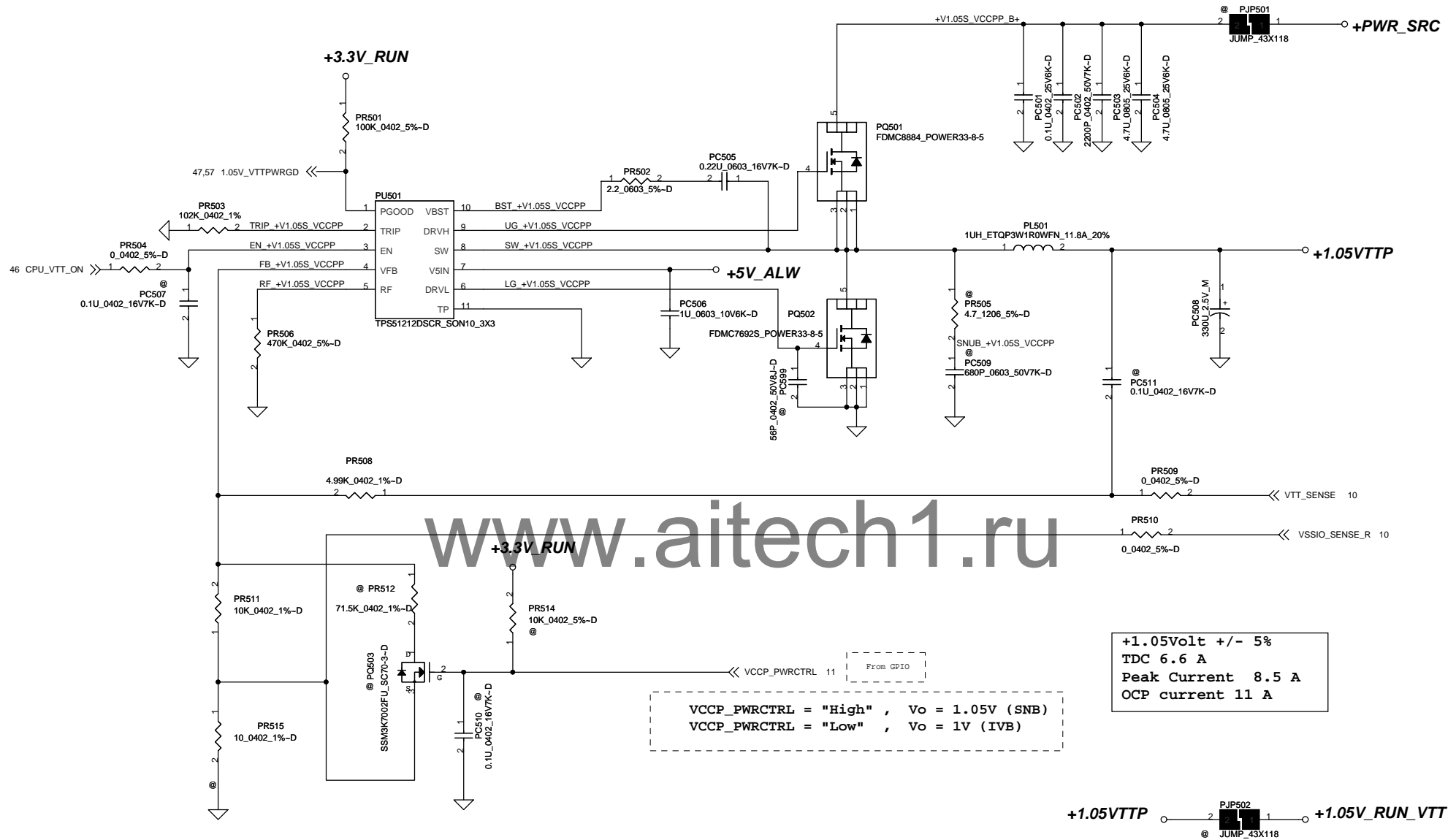


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Size	Document Number	LA-7933	
Date	Monday, November 07, 2011	Sheet	55 of 65
Rev		0.2	

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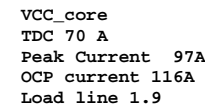
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Size	Document Number	LA-7933	
Date	Monday, November 07, 2011	Sheet	56 of 65
		Rev	0.2







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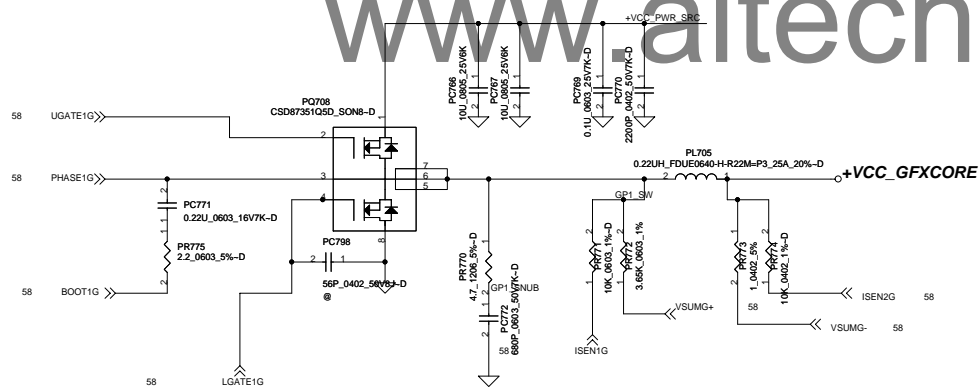
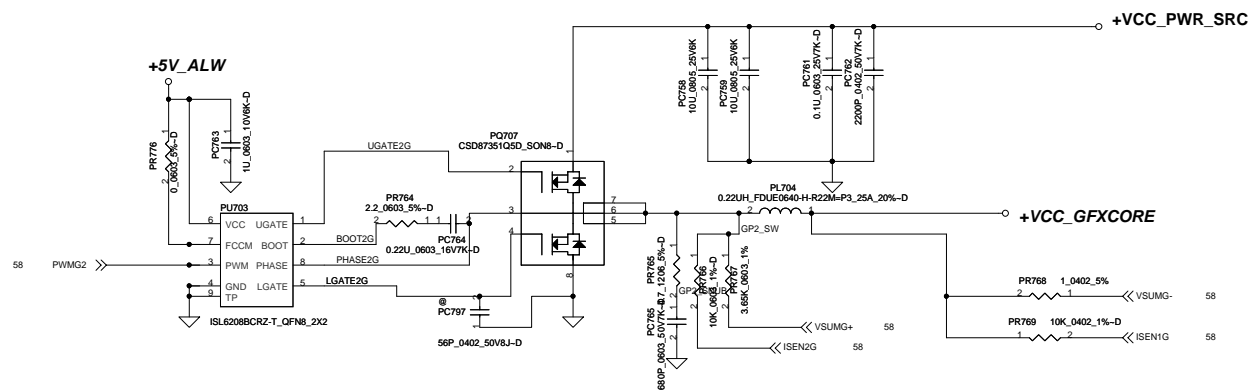
**+VCC\_CORE**

LA-7933

Date: \_\_\_\_\_ Sheet 58 of 65

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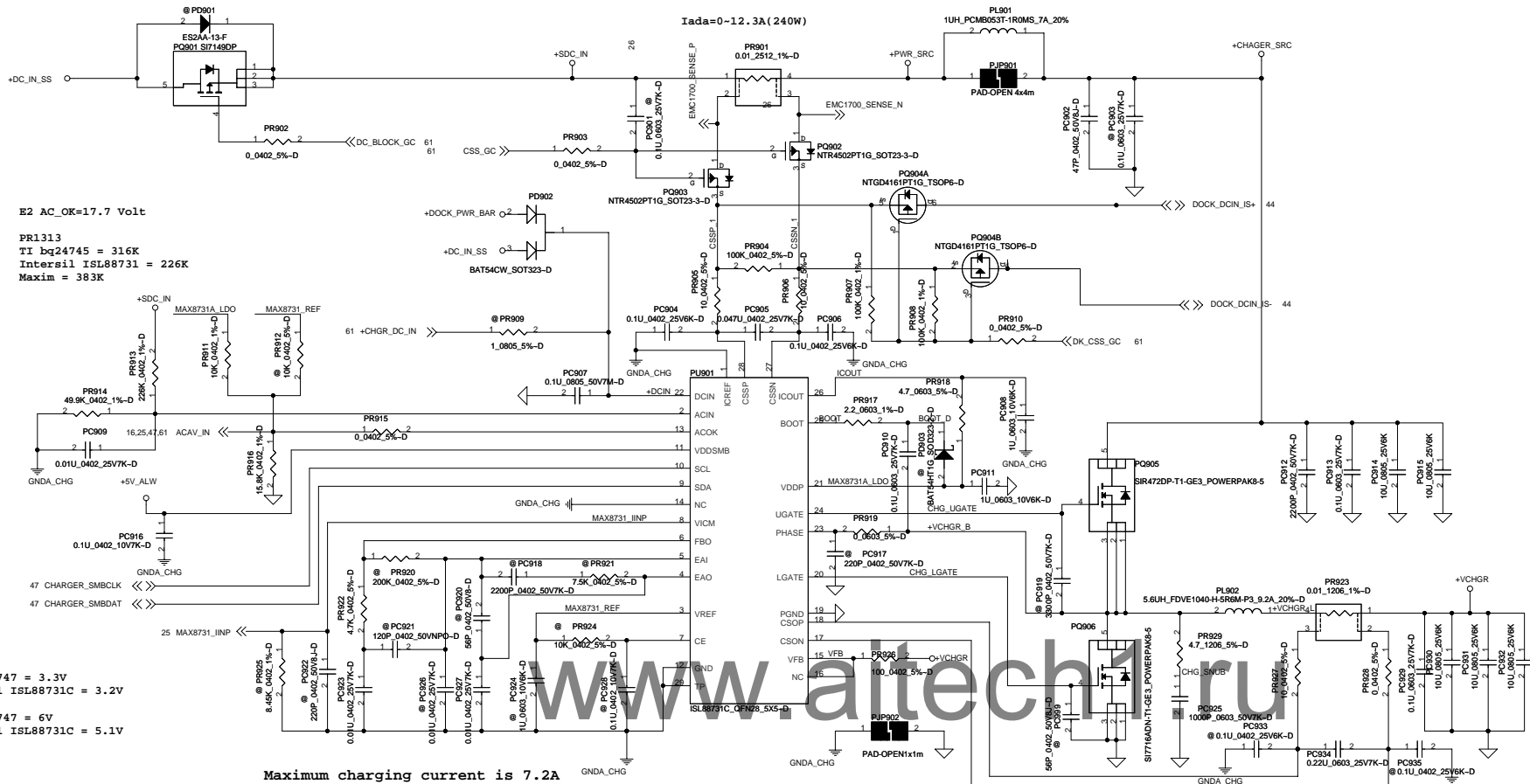
VCC\_GFXCORE  
TDC 38A  
Peak Current 50A  
OCP current 57.18A  
Load line 3.9



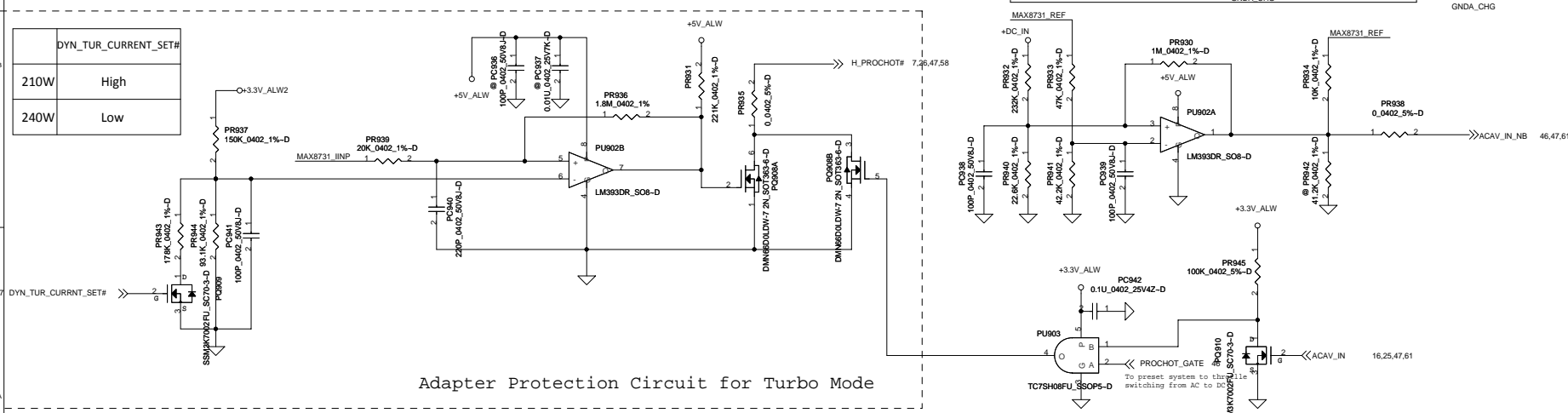
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File		+VCC_GFXCORE	
Size	Document Number	LA-7933	
Date:	Sheet	59	of 65
		Rev	0.2



DYN_TUR_CURRENT_SET#	
210W	High
240W	Low



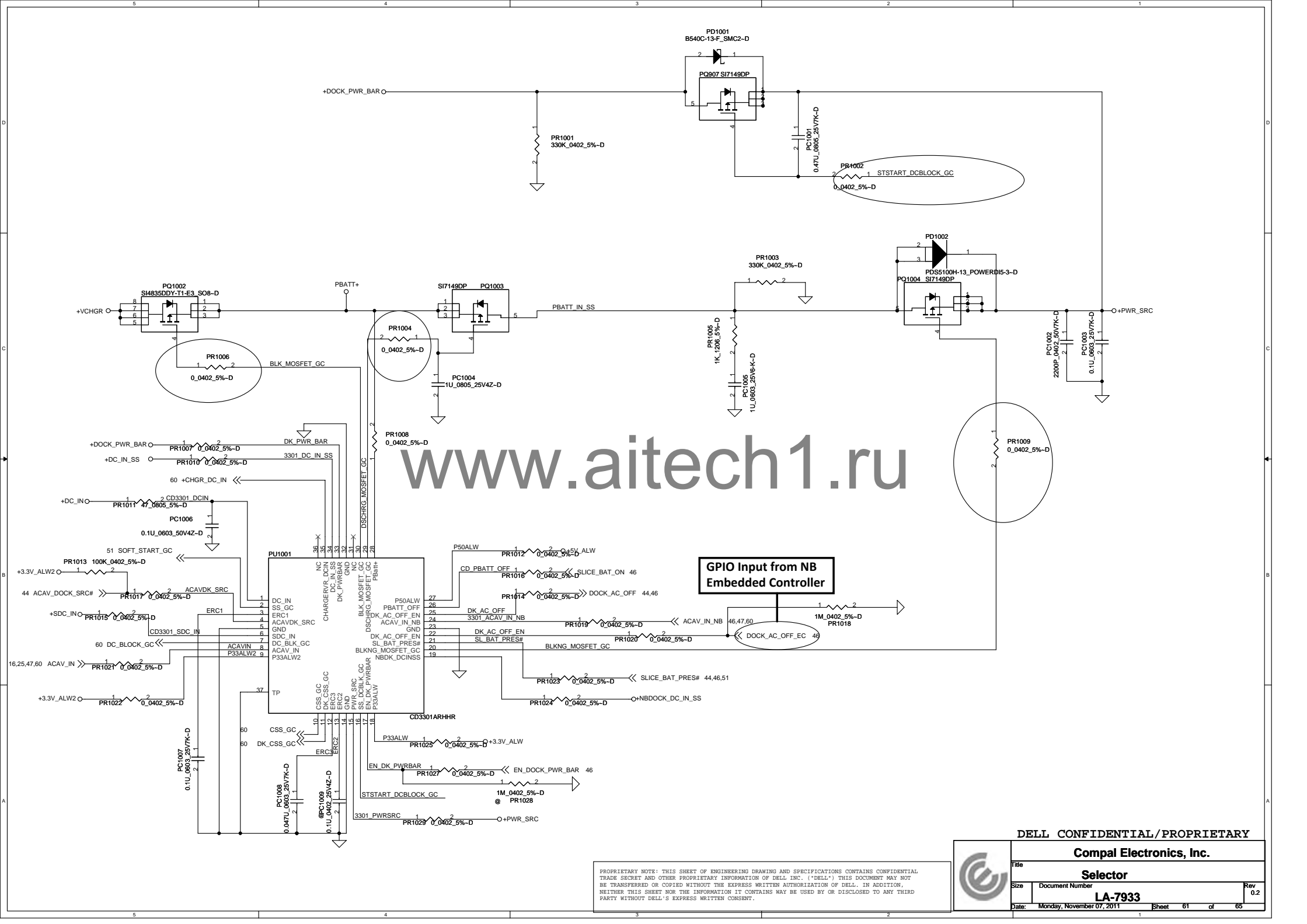
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Charger

File	Document Number	Rev
Size	LA-7933	0.2
Date	Monday, November 07, 2011	Sheet 60 of 65



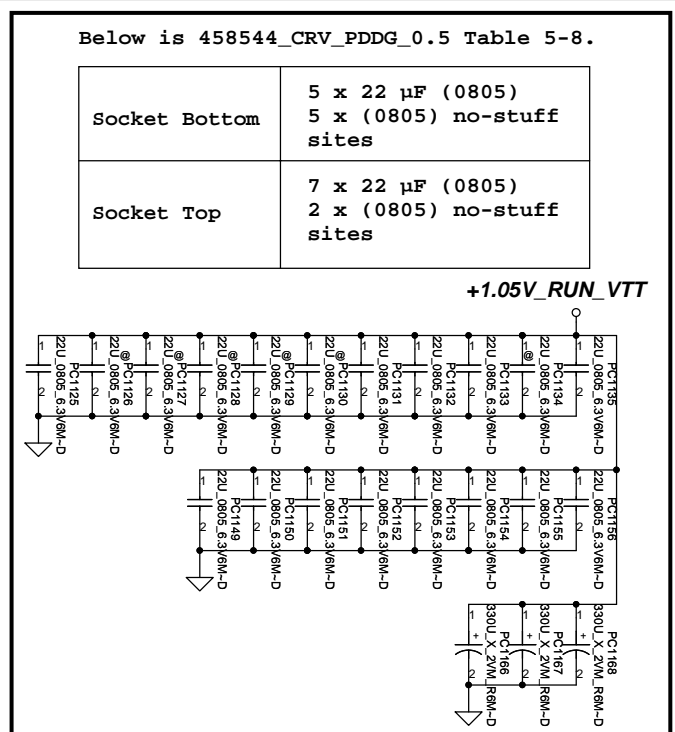
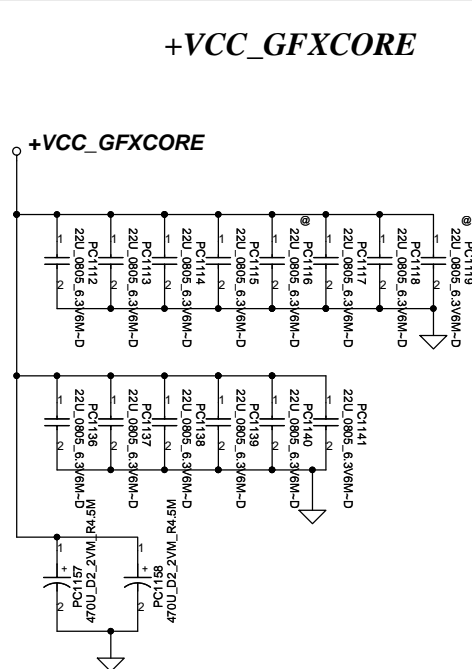
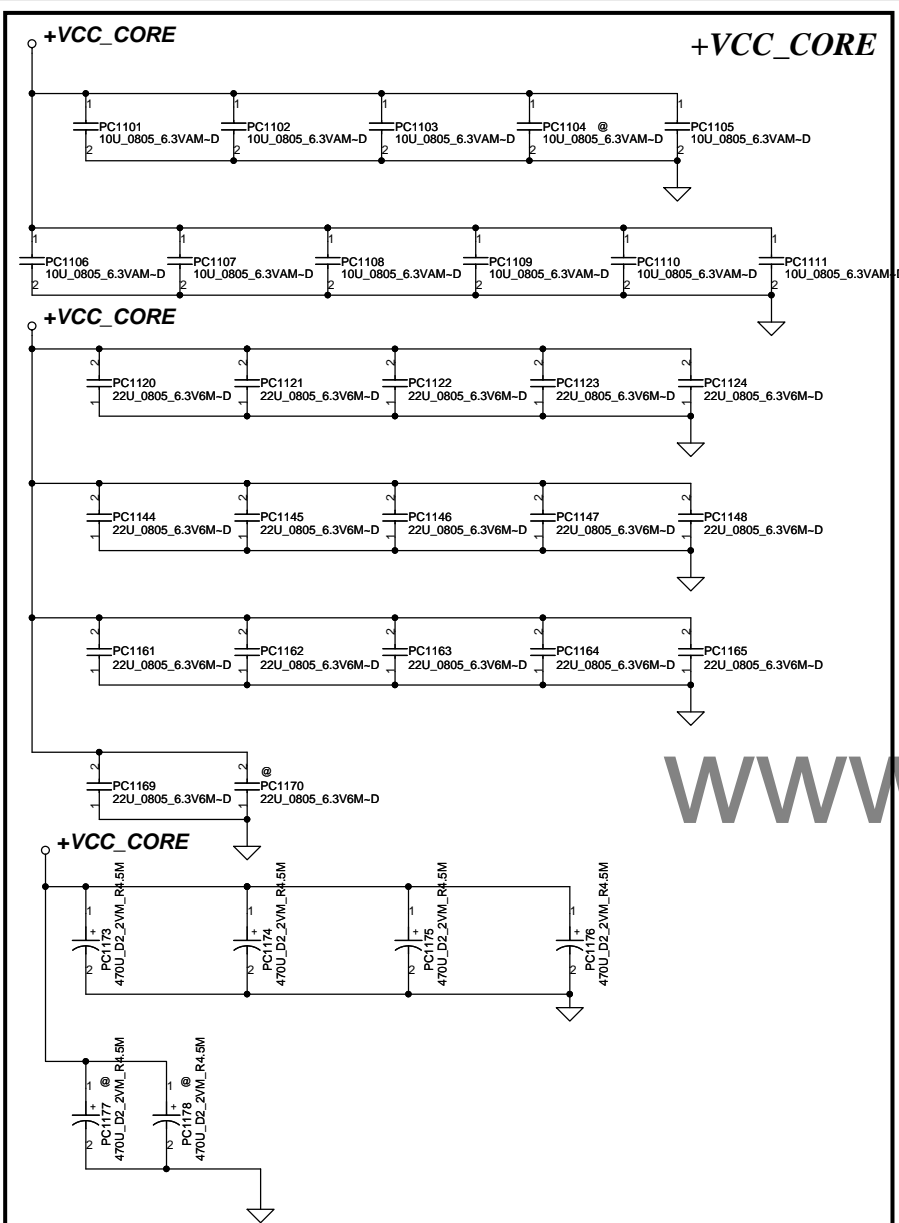
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Title		
Selector		
LA-7933		
Size	Document Number	Rev
		0.2
Date: Monday, November 07, 2011		
Sheet	61	of 65



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Title		Rev 0.2
Size	Document Number LA-7933	
Date	Monday, November 07, 2011	Sheet 62 of 65

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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	60	PWR	10/11	Intersil	Modify docking current sense feedback to PU901 CSSP and CSSN connection	Modify PR946, PR948 and PR947 connection	X01
2	51	PWR	10/13	Compal	Change RTC battery connector	Change to SP02000R000	X01
3	51	PWR	10/13	Compal	Add control singnal to control S5 power consumption	Add PR23 to connect PCH_ALW_ON singal	X01
<del>4</del>	<del>60</del>	<del>PWR</del>	<del>10/14</del>	<del>Compal</del>	<del>Change H_PROCHOT# voltage source of Compare reference</del>	<del>PR937 connect to 2VREF_6182</del>	<del>X01</del>
5	51	PWR	10/25	Compal	Change PQ5 Package for layout space	Change footprint from T0252 to S08_5P	X01
6	60	PWR	10/28	Intersil	Remove Docking current sense voltage division	Remove PR946, PR948 and PR947	X01
7	58	PWR	11/01	Compal	Change PC707 PC751 footprint from 0603 to 0402	Change PC707 PC751 footprint to 0402	X01
8	59	PWR	11/01	Compal	Remove PJP902	Remove PJP902	X01
9	52,53,55, 56,58,59, 60	PWR	11/07	Compal	Low side MOSFET Gate induce voltage	Reserve PC198,PC199,PC299,PC499,PC599,PC791,PC792, PC793,PC794,PC795,PC796,PC797,PC798,PC999	X01
10	51	PWR	11/07	Compal	Reserve 10u and 0.1u Cap with MXM_pwr_src	Reserve PC30 and PC31	X01

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Compal Electronics, Inc.		
Title <b>PWR_PIR 1</b>		
Size	Document Number <b>LA-7933</b>	Rev 0.2
Date: Monday, November 07, 2011	Sheet 63	of 65

# Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	49	HW	9/23/2011	COMPAL	to meet LED min workable current(2mA).	Change R934,R939,R942,R955,R941 from 2.2kohm to 1.2kohm. R943 from 2.2kohm to 374ohm.	0.2(X01)
2	49	HW	9/23/2011	COMPAL	Breath LED Lose current-limited resistors	Add R956	0.2(X01)
3	26	HW	9/23/2011	DELL	For cost saving	No stuff U5,C17,C363,R1975 U6,C16,C361,R1974	0.2(X01)
4	47	HW	9/23/2011	COMPAL	Code change	U54 change from SA00003TZ2L to SA00003TZ1L	0.2(X01)
5	16	HW	9/23/2011	COMPAL	correct MXM LVDS signals.	Swap CHA and CHB signals on JMXM1.	0.2(X01)
6	32	HW	10/04/2011	COMPAL	Add DOCK DPB DDC signals control circuit.	Stuff C1174,R1532,R1537,R1530,R1539,Q110,Q113	0.2(X01)
7	33	HW	10/04/2011	COMPAL	Add DOCK DPA DDC signals control circuit.1/2	Add C1332,R2151-R2153,R2155-R2157,Q335,Q336	0.2(X01)
8	50	HW	10/04/2011	COMPAL	+3.3V_RUN boot leakage	Pop R929,Q69	0.2(X01)
9	33	HW	10/04/2011	COMPAL	Change the R518 value to meet the PS8336B input high-level voltage.	Change R518 from 100k to 10kohm.	0.2(X01)
10	50	HW	10/04/2011	COMPAL	Solve S4/S5 +MXM_PWR_SRC leakage in DC mode.	Change R940 pin1 connect from +PWR_SRC_S to +PWR_SRC_MXM.	0.2(X01)
11	30	HW	10/05/2011	COMPAL	Due to LVDS and eDP use same connector . It will easy to damage on MB or panel when install wrong 40pin connector for LVDS and eDP	Change eDP pin defined same as LVDS	0.2(X01)
12	30	HW	10/05/2011	COMPAL	Q13 VGS voltage limit of ±20V	Change R162 pin1 connect from +PWR_SRC_S to +3.3V_ALW.	0.2(X01)
13	17,18,47 36	HW	10/05/2011	COMPAL	Crystal BA.	Change C743,C741 from 22pF to 39pF, CH2,CH3 from 15pF to 18pF, CH18,CH19 from 12pF to 10pF, C470 from 33pF to 22pF, C471 from 33pF to 27pF	0.2(X01)
14	46	HW	10/12/2011	COMPAL	Wireless switch needs to be pulled to ALW, Without it being pulled to ALW rail AOAC will not work correct.	Add R2158 let WIRELESS_ON#/OFF pull up to ALW, no stuff R766	0.2(X01)
<del>15</del>	<del>49</del>	<del>HW</del>	<del>10/13/2011</del>	<del>COMPAL</del>	<del>Solve Breath LED flicker when AC in plug and correct Breath LED top and side view work behavior.</del>	<del>Add Q327 and use"MASK_BASE_LEDS#" to control Breath LED top view. use"SVG_LED_MASK#" to control Breath LED side view.</del>	<del>0.2(X01)</del>
16	48	HW	10/13/2011	COMPAL	To meet intel spec:T235(power off)=min40ns). T08a(power on)= max 90ms.	change U4 from RT9801AGE to RT9818A-44GU3,R1622 to 100kohm.add R2159. remove R1649~R1654 pop R1633,non-pop R1623	0.2(X01)
17	44,28,30 45,25,12	ME	10/13/2011	COMPAL	Change connector follow connector list 0913A and 1005A.	Change JDock1 to WD2F144WB5R400,JLVDS1,JEDP1 to 50398-04071-001,JPB1 to 50228-0067N-001. JFAN1 & JFAN2 to 50271-0040N-001, JDIMM1 to 2-2013311-1	0.2(X01)
18	48	HW	10/20/2011	COMPAL	To avoid layout trace width less to 10mil	Add U4.1 net name of +5V_ALW_PCH_R	0.2(X01)
<del>19</del>	<del>28,30</del>	<del>HW</del>	<del>10/20/2011</del>	<del>COMPAL</del>	<del>Avoid JEDP1 and JLVDS1 insert anti burn panel from +BL_PWR_SRC</del>	<del>Q22.2 connector to JEDP1.11</del>	<del>0.2(X01)</del>
20	40	HW	10/25/2011	COMPAL	TPM chip to new version chip due to OS Win8 supported problem	Change U39 TPM solution to new p/n: SA00004WQ10	0.2(X01)
21	44	HW	10/25/2011	COMPAL	Audio not transfer to DP display if play movie when attached external DP display	Add pull down 100K on MXM_DPB_HPD of R2160	0.2(X01)

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Title EE P.I.R (1/2)			Rev 0.2
Size	Document Number LA-7933		
Date Monday, November 07, 2011	Sheet 64	of 65	

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# Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
22	49	HW	10/25/2011	COMPAL	BT LED will be light when system is in S3/S4/S5	We change R938 PU from +3.3V_RUN to +3.3V_ALW and It can fix this issue.	0.2(X01)
23	50	HW	10/26/2011	COMPAL	For smart card detect failed	For +3.3V_SUS power sequence.Change C767 from 4700pF to 470pF	0.2(X01)
24	50	HW	10/26/2011	COMPAL	For Inrush current issue	Modify +5V_RUN/+3.3V_RUN soft start.Change C777 from 470pF to 2200pF	0.2(X01)
25	49	HW	10/26/2011	COMPAL	Breath LED need to add control schematics	Remove Q327 and modify EC code from PWM Output to GPIO input on ECE5048(GPIOM3/PWM4) which follow E4 solution.	0.2(X01)
26	22	HW	10/26/2011	COMPAL	CRT ripple garbage display issue. 1/2	change LH1 to 1uH inductor.	0.2(X01)
27	39	DFB	10/27/2011	COMPAL	DFB Suggest to relocate L41,L43,L44 from bottom to top side.	In order to trace along the line of the L41,L43,L44 reverse	0.2(X01)
28	49	HW	10/27/2011	COMPAL	Schematic error, let H26, H27,H28,H29 all have two location(H22, H23, H24, H25) in the CAD file	Remove H26,H27,H28,H29	0.2(X01)
29	44	HW	11/01/2011	COMPAL	EMI request,add 33ohm for DOCK DVI signals.	Add R2164~R2179(33ohm) for DOCK DVI port A,B.	0.2(X01)
30	22	HW	11/02/2011	COMPAL	CRT ripple garbage display issue. 2/2	Add CH37 of 10U 0603	0.2(X01)
31	21	HW	11/02/2011	COMPAL	PCH has internal pull up 20k ohm on (GPIO27)	No stuff RH175	0.2(X01)
32	21	HW	11/02/2011	COMPAL	Power saving	RH179 change from 10K to 100K	0.2(X01)
33	33	HW	11/02/2011	COMPAL	EMI request and HDMI EA have verify it.	Pop R451~R456,R458,R459 and non-pop L19,L23~25 R74 change from 4.99k to 5.76K for reduce swing.	0.2(X01)
34	47	HW	11/02/2011	COMPAL	Change board ID to X01	Change R875 to 130K	0.2(X01)
35	50	HW	11/02/2011	COMPAL	Power saving	R935 change from 20K to 100K	0.2(X01)
36	40	HW	11/02/2011	COMPAL	U39.14 internal is empty pin	No stuff C554	0.2(X01)
37	20	HW	11/02/2011	COMPAL	Avoid WWAN noise affect PCI 3,3M CLK.	Add CH21~23 by pass cap.	0.2(X01)
38	39	HW	11/02/2011	COMPAL	For ESD request.	D14,D16 change main source SC30000250L to SC300002F0L	0.2(X01)
39	49	ME	11/03/2011	COMPAL	ME drawing modify	Remove H21 and H10 from 3P3 to 3P0	0.2(X01)
40	44	HW	11/03/2011	COMPAL	For ESD request.	Non-pop D33,D10,D11	0.2(X01)
41	37	HW	11/03/2011	COMPAL	Vendor service issue	Change T156 from P050005A0L(PULSE) to SP050006P0L(TAIMAG)	0.2(X01)
42	33	HW	11/03/2011	COMPAL	Add DOCK DPA DDC signals control circuit.2/2	Add R2154,R2161,R2162,R2163,Q337 but no stuff	0.2(X01)
43	33	HW	11/04/2011	COMPAL	EMI request,add reserve C(3.3pF) for HDMI signals.	Add reserve C1333~C1340(3.3pF) for HDMI signals.	0.2(X01)
44	31	LAYOUT	11/08/2011	COMPAL	Add TEST point for JCRT PIN11.	Add CRT_11 net and test point(T61) for JCRT1.11.	0.2(X01)
45	07	HW	11/08/2011	COMPAL	Avoid Power_SRC trace noise coupling effect to CPU	Add CC92	0.2(X01)
46	26,50	HW	11/09/2011	DELL	For DELL request add Monitor PWR_SRC MXM circuit by HW control	Remove R1973, add PJP78,79 Remove U5,C17,C363,R1975,R1181,R20,U6,C16,C361,R1974,R19 Add U59,PU2,PQ1005,PR14,PR24~31,PC6,PC17~21 and no stuff	0.2(X01)
47	44	HW	11/11/2011	COMPAL	For DP EA consider	Change R2164~R2179(33ohm) to 0ohm	0.2(X01)
48	39	HW	11/11/2011	COMPAL	For USB EA JUSB1 ,Need to pop R24/R15/R18 JUSB2 ,Need to pop R33/R27/R29	Pop R15,R27	0.2(X01)

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Title	EE P.I.R (1/2)	
Size	Document Number	Rev
	LA-7933	0.2
Date:	Friday, November 11, 2011	Sheet 65 of 65